V6300 Datasheet

Version: 0.2
Release Date: September 15, 2016

Specifications are subject to change without notice.

Revision History

Date	Version	Description
2016.07.15	0.1	Initial release
2016.09.15	0.2	Specified V6300 accompanied with V6000 (Driving capability: 4 A)

General Description

The V6300 is a narrowband Power Line Communication (PLC) processor chip. The V6300 integrates one 32-bit MCU, one 32-bit DSP, one embedded Flash memory, two UART interfaces, one SPI Master controller, one SPI Slave interface, one I^2C Master interface, PLC MAC/PHY layer functions, and Analog Front-End (AFE). Accompanied with Vango's high-current drive line driver chip (V6000), the V6300 forms a complete modem solution to support all known narrowband PLC Standards.

Features

- Supporting multiple narrowband PLC Standards: G3-PLC, IEEE P1901.2, PRIME, ITU-T G.hnem; also supporting single-carrier or multi-carrier PLC with FSK or BPSK/DBPSK modulation schemes
- With high-linearity and high-current drive line driver (V6000) having integrated receive functions, it offers the lowest BOM cost for G3-PLC/PRIME standards.
- Supporting frequency bands: CENELEC, FCC, and ARIB
- Supporting modulations: Selectable differential and coherent BPSK, QPSK, 8PSK, and coherent 16QAM
- Supporting IPv6 networking layer
- Supporting G3-PLC compliant 6LoWPAN adaptation layer with optimized network formation and mesh routing function
- Supporting HW AES-128
- Two UART interfaces (UART0 and UART1). UART1 is high-speed UART supporting up to 500-Kbps baud rate.
- One SPI Master with two chip select pins. It can be used to control wireless transceiver, metering, or other SPI devices.
- One SPI Slave interface for alternative data interface with Master processor chip
- One I^2C Master interface to control other I^2C devices
- 256-KB embedded Flash memory
- Supporting In-System Programming (ISP) of Flash memory via UART0 or SPI Slave interface
- Up to 32 programmable GPIOs for maximal flexibility
- 3.3-V digital I/O. UART pins are 5 V tolerant.
- Integrated LDO (3.3 V to 1.2 V)
- Packages:
  - V6300P: 80-pin T/LQFP
  - V6300N: 68-pin QFN
- Operating temperature: -40 °C ~ +85 °C

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1. Electrical Characteristics

1.1. Absolute Maximum Ratings

While the operating circumstance exceeding "Absolute Maximum Ratings", it may cause the permanent damage to the device.

Table 1-1 Absolut Maximum Ratings

Parameter	Min.	Max.	Unit	Description
AVDD33, DVDD33, 3V3_IN Pins	-0.5	+3.6	V	Relative to ground
DVDD12 Pins	-0.5	+3.6	V	Relative to ground
I/O Pins	-0.5	+3.6	V	Relative to ground
UART I/O Pins	-0.5	+5.5	V	Relative to ground
Operating Temperature	-40	+85	°C	
Storage Temperature	-40	+125	°C	
Junction Temperature	-	125	°C	
Lead Temperature (Soldering, 10s)	-	300	°C	

1.2. Electrical Characteristics

All maximum and minimum specifications apply to the entire recommended operation range (T = -40 °C ~ 85 °C), unless otherwise noted. All typical specifications are at TA = 25 °C.

Table 1-2 Electrical Characteristics Table

Parameter	Min.	Typ.	Max.	Unit	Description
3.3V Supply Voltage (AVDD33, DVDD33 pins)	3.0	3.3	3.6	V	
1.2V Supply Voltage (DVDD12 pins)	1.08	1.2	1.32	V	
Operating Current (DVDD33)		10		mA	
Operating Current (AVDD33)		25		mA	
Operating Current (DVDD12)		120	160	mA	
Integrated 3.3V to 1.2V LDO					

Parameter	Min.	Typ.	Max.	Unit	Description
3V3_IN	2.0	3.3	3.6	V	3.3 V input of LDO
1.2 V Output	1.14	1.2	1.26	V	1.2 V output (to supply DVDD12)
Load Current driving capacity			220	mA	Load current should not be over the maximum driving capacity
Digital IO, Output					
Output High Voltage, V_{OH}	2.4			V	
I_{SOURCE}		4	16	mA	
Output Low Voltage, V_{OL}			0.4	V	
I_{SINK}		4	16	mA	
Digital IO, Input					
Input High Voltage, V_{IH}	2.0			V	
Input Low Voltage, V_{IL}			0.8	V	
GPIO Pull Up/Down Resistance		75		KΩ	
5V tolerance I/O output pull-up voltage		2.29		V	I_{pu} = 1.0 uA

1.3. Flash Memory Specifications

All maximum and minimum specifications apply over the entire recommended operation range (T = -40 °C ~ 85 °C), unless otherwise noted. All typical specifications are at TA = 25 °C.

Table 1-3 Flash Memory Specifications

Parameter	Min.	Typ.	Max.	Unit	Description
Flash Memory					
Read Access Time			25	ns	DVDD12= 1.12~1.32 V
Endurance	20000			cycle	-40 °C ~ +85 °C
Data Retention	10			year	85 °C
Page Write Time			2	ms	
Page Erase Time (512 bytes)			3	ms	

Parameter	Min.	Typ.	Max.	Unit	Description
Mass Erase Time			3	ms	

1.4. SPI Timing Specifications

All maximum and minimum specifications apply to the entire recommended operation range (T = -40 °C ~ +85 °C), unless otherwise noted.

Table 1-4 Master SPI (MSPI) Timing Specifications

Parameter		Min.	Max.	Unit
f_{MSPI}	MSPI_CLK frequency		8	MHz
t_{MCYC}	MSPI_CLK cycle time	$1/f_{MSPI}$		ns
t_{MPH}	MSPI_CLK pulse high	$1/(2f_{MSPI})-5$		ns
t_{MPL}	MSPI_CLK pulse low	$1/(2f_{MSPI})-5$		ns
t_{MVLD}	MSPI_MOSI valid time after SPI_CLK rising	$1/(2f_{MSPI})$		ns
t_{MSETUP}	MSPI_MISO setup time before SPI_CLK rising	5		ns
t_{MHOLD}	MSPI_MISO hold time after SPI_CLK rising	5		ns
t_{MCS_SETUP}	MSPI_CS setup time before SPI_CLK rising	$1/f_{MSPI}$		ns
t_{MCS_HOLD}	MSPI_CS hold time after SPI_CLK falling	$1/f_{MSPI}$		ns

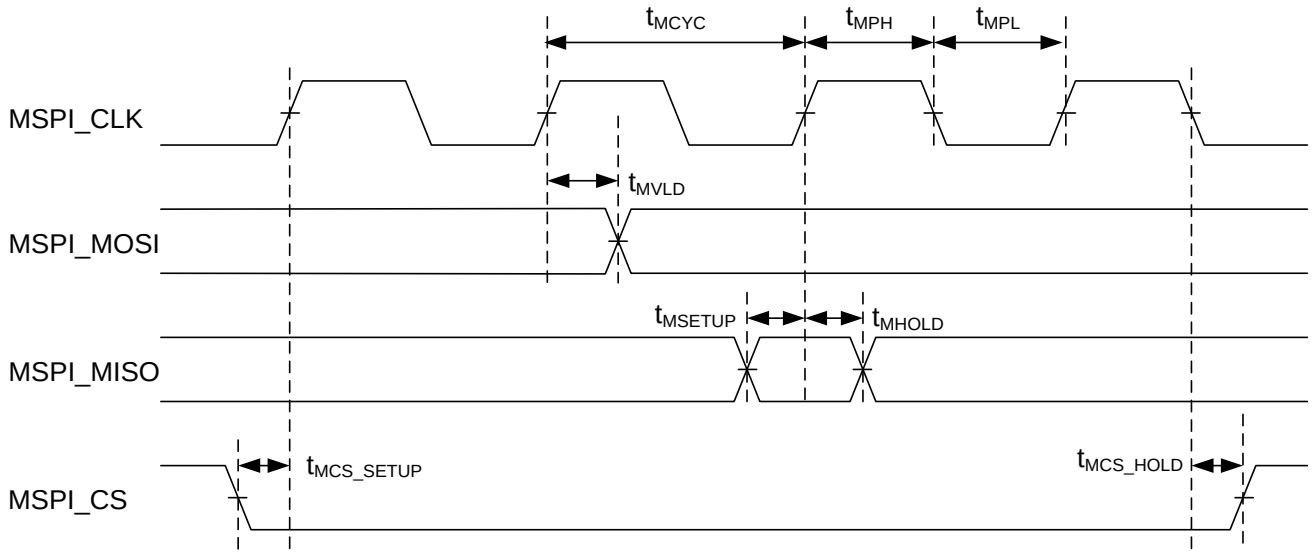


Figure 1-1 MSPI Timing Diagram

Table 1-5 Slave SPI (SSPI) Timing Specifications

Parameter		Min.	Max.	Unit
f_{SSPI}	SSPI_CLK frequency		8	MHz
t_{SCYC}	SSPI_CLK cycle time	$1/f_{SSPI}$		ns
T_{SPH}	SSPI_CLK pulse high	$1/(2f_{SSPI})-5$		ns
t_{SPL}	SSPI_CLK pulse low	$1/(2f_{SSPI})-5$		ns
t_{SVLD}	SSPI_MISO valid time after SSPI_CLK rising	$1/(2f_{SSPI})$		ns
T_{SSETUP}	SSPI_MOSI setup time before SSPI_CLK rising	5		ns
T_{SHOLD}	SSPI_MOSI hold time after SSPI_CLK rising	5		ns
T_{SCS_SETUP}	SSPI_CS setup time before SSPI_CLK rising	$1/f_{SSPI}$		ns
t_{SCS_HOLD}	SSPI_CS hold time after SPI_CLK falling	$1/(2f_{SSPI})$		ns

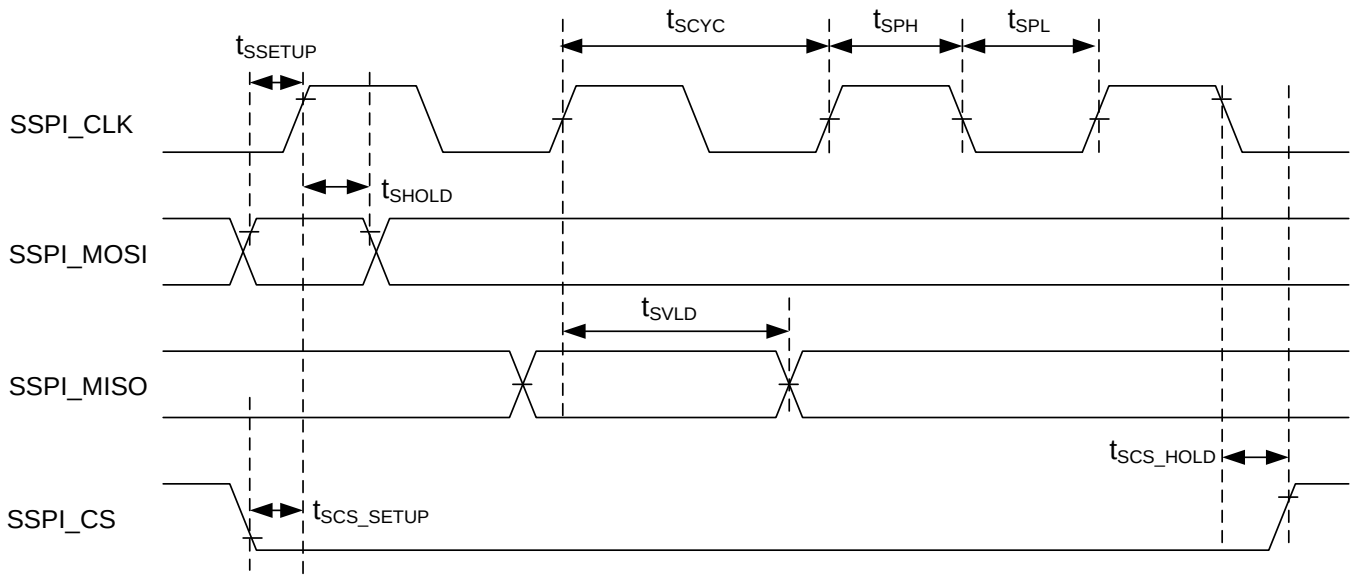


Figure 1-2 SSPI Timing Diagram

2. Pin Descriptions

68L-QFN

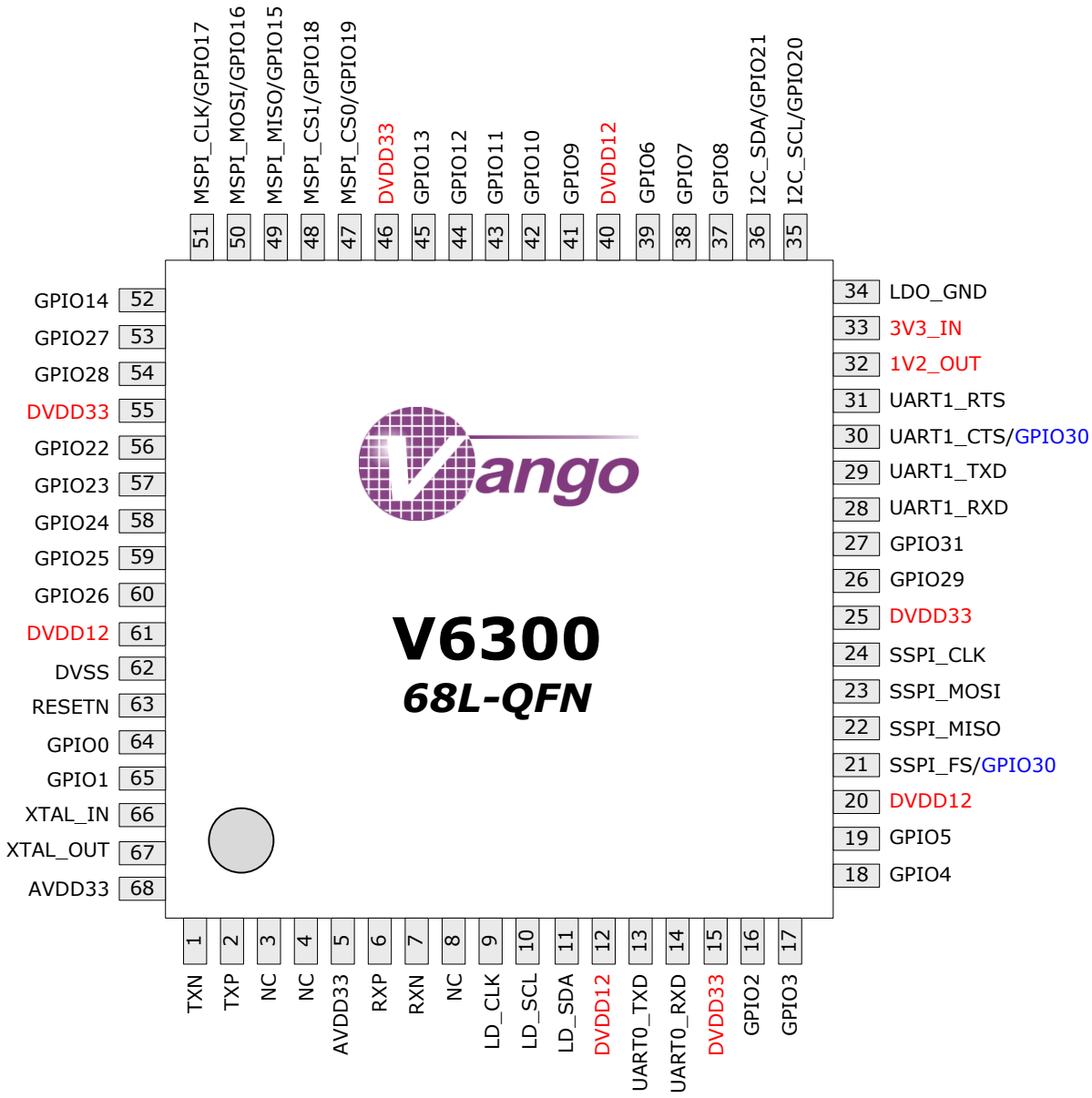


Figure 2-1 68L-QFN Pin Assignments

Table 2-1 68L-QFN Pin Descriptions

(Pin type: "O"=Output, "I"= Input, "P"=Power, "G"=Ground)

No.	Mnemonic	Type	Description
1	TXN	O	DAC differential output (Negative) to Line Driver chip (V6000).
2	TXP	O	DAC differential output (Positive) to Line Driver chip (V6000).
3	NC		NC. Always keep floating.
4	NC		NC. Always keep floating.
5	AVDD33	P	Analog 3.3V power.
6	RXP	I	ADC differential input (Positive) from Line Driver chip (V6000).
7	RXN	I	ADC differential input (Negative) from Line Driver chip (V6000).
8	NC		NC
9	LD_CLK	O	Clock output to Line Driver chip (V6000).
10	LD_SCL	O	Line driver (V6000) control interface clock output.
11	LD_SDA	I/O	Line driver (V6000) control interface data.
12	DVDD12	P	Digital 1.2V power.
13	UART0_TXD	O	Low-Speed UART port 0: data output. Support baud rate from 1200 to 115200 bps. 5V tolerant.
14	UART0_RXD	I	Low-Speed UART port0: data input. Support baud rate from 1200 to 115200 bps. 5V tolerant.
15	DVDD33	P	Digital 3.3V power.
16	GPIO2	I/O	General Purpose I/O.
17	GPIO3	I/O	General Purpose I/O.
18	GPIO4	I/O	General Purpose I/O.
19	GPIO5	I/O	General Purpose I/O.
20	DVDD12	P	Digital 1.2V power.
21	SSPI_FS GPIO30	I I/O	Slave SPI frame sync input. General Purpose I/O. GPIO30 can be used either on pin 21 or pin 30.

22	SSPI_MISO	O	Slave SPI data output.
23	SSPI_MOSI	I	Slave SPI data input.
24	SSPI_CLK	I	Slave SPI clock input
25	DVDD33	P	Digital 3.3V power.
26	GPIO29	I/O	General Purpose I/O.
27	GPIO31	I/O	General Purpose I/O.
28	UART1_RXD	I	High-speed UART port 1: data input. Support baud rate from 1200 to 500K bps. 5V tolerant.
29	UART1_TXD	O	High-speed UART port 1: data output. Support baud rate from 1200 to 500K bps. 5V tolerant.
30	UART1_CTS GPIO30	O I/O	High-speed UART port 1: Clear to Send. General Purpose I/O. GPIO30 can be used either on pin 21 or pin 30. 5V tolerant.
31	UART1_RTS	I	High-speed UART port 1: Request to Send. 5V tolerant.
32	1V2_OUT	P	Internal LDO 1.2V output. It must be tied to all the 1.2V power pin of V6300
33	3V3_IN	P	Internal LDO 3.3V input.
34	LDO_GND	G	Internal LDO ground.
35	I2C_SCL GPIO20	O I/O	Host I2C port serial clock General Purpose I/O.
36	I2C_SDA GPIO21	I/O I/O	Host I2C port serial data General Purpose I/O.
37	GPIO8	I/O	General Purpose I/O.
38	GPIO7	I/O	General Purpose I/O.
39	GPIO6	I/O	General Purpose I/O.
40	DVDD12	P	Digital 1.2V power.

41	GPIO9	I/O	GPIO9: General Purpose I/O.
42	GPIO10	I/O	GPIO10: General Purpose I/O.
43	GPIO11	I/O	GPIO11: General Purpose I/O.
44	GPIO12	I/O	GPIO12: General Purpose I/O.
45	GPIO13	I/O	GPIO13: General Purpose I/O.
46	DVDD33	P	Digital 3.3V power.
47	MSPI_CS0 GPIO19	O I/O	Master SPI select 0 General Purpose I/O.
48	MSPI_CS1 GPIO18	O I/O	Master SPI select 1 General Purpose I/O.
49	MSPI_MISO GPIO15	I I/O	Master SPI data input General Purpose I/O.
50	MSPI_MOSI GPIO16	O I/O	Master SPI data output General Purpose I/O.
51	MSPI_CLK GPIO17	O I/O	Master SPI clock output General Purpose I/O.
52	GPIO14	I/O	General Purpose I/O.
53	GPIO27	I/O	General Purpose I/O.
54	GPIO28	I/O	General Purpose I/O.
55	DVDD33	P	Digital 3.3V power.
56	GPIO22	I/O	General Purpose I/O.
57	GPIO23	I/O	General Purpose I/O.
58	GPIO24	I/O	General Purpose I/O.
59	GPIO25	I/O	General Purpose I/O.
60	GPIO26	I/O	General Purpose I/O.
61	DVDD12	P	Digital 1.2V power.
62	DVSS	G	Must be tied to GND.
63	RESETN	I	Reset input (Active low). It should be pulled low at least 100ms for reset period after power on.
64	GPIO0	I/O	General Purpose I/O.

65	GPIO1	I/O	General Purpose I/O.
66	XTAL_IN	I	Input of Crystal oscillator driver. (24MHz)
67	XTAL_OUT	O	Output of Crystal oscillator driver.
68	AVDD33	P	Analog 3.3V power.
	EPAD	G	Must be tied to GND.

80L-T/LQFP

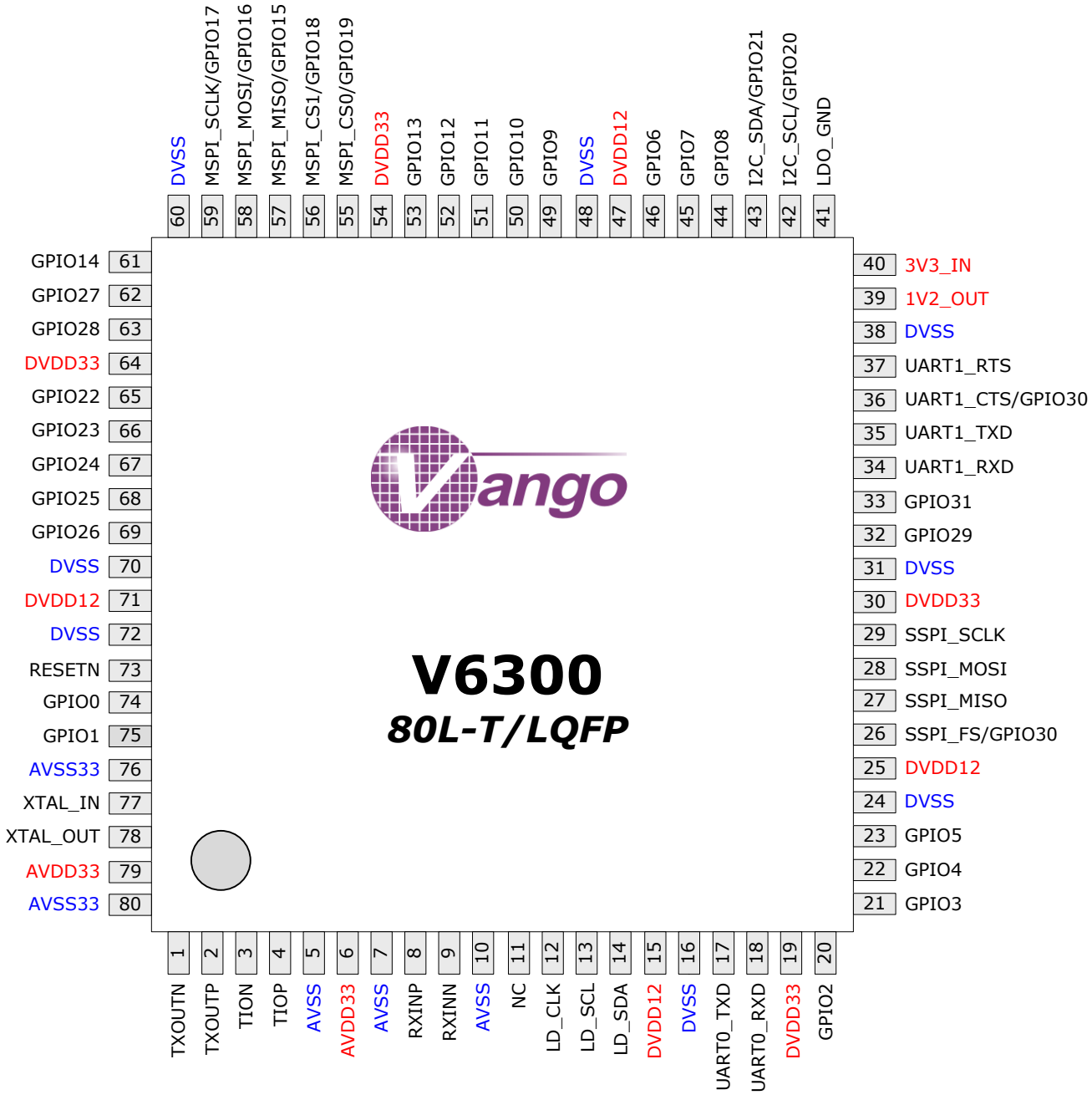


Figure 2-2 80L-T/LQFP Pin Assignments

Table 2-2 80L-T/LQFP Pin Descriptions

(Pin type: "O"=Output, "I"= Input, "P"=Power, "G"=Ground)

No.	Mnemonic	Type	Description
5,7,10,76,80	AVSS	P	Analog ground.
16,24,31,38,48,60,70,72	DVSS	G	Digital ground.

Note: Except power/ground pins, signal pins are the same as 68L-QFN. Please refer to 68L-QFN Pin Descriptions.

3. Functional Block Diagram

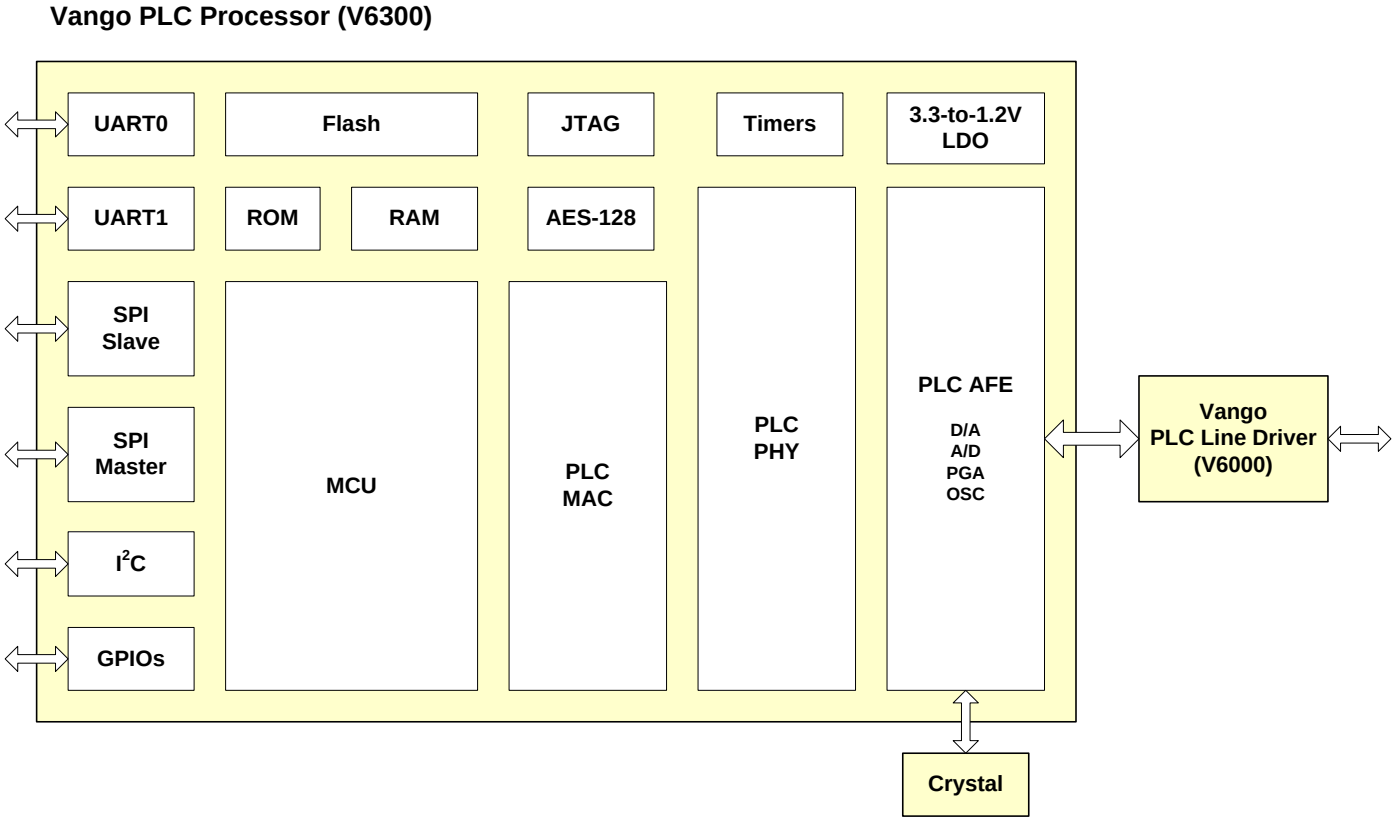


Figure 3-1 Functional Block Diagram

4. System Block Diagram

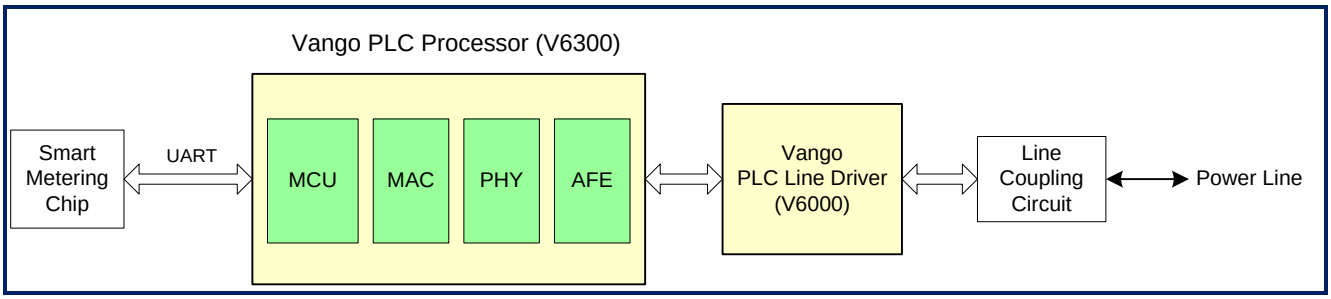


Figure 4-1 System Block Diagram of Leaf Node Application Example

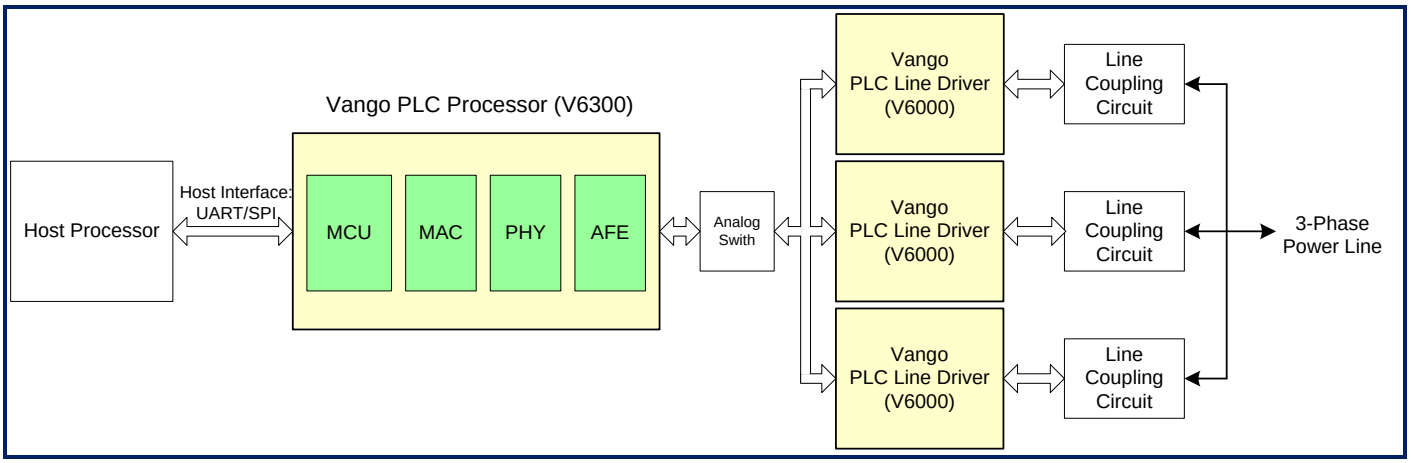


Figure 4-2 System Block Diagram of Concentrator Application Example

5. Power Supply

Figure 5-1 shows the power supply architecture of V6300. The integrated LDO (3.3V to 1.2V) is used to generate 1.2V supply voltage to DVDD12 to reduce the BOM cost of power supply components.

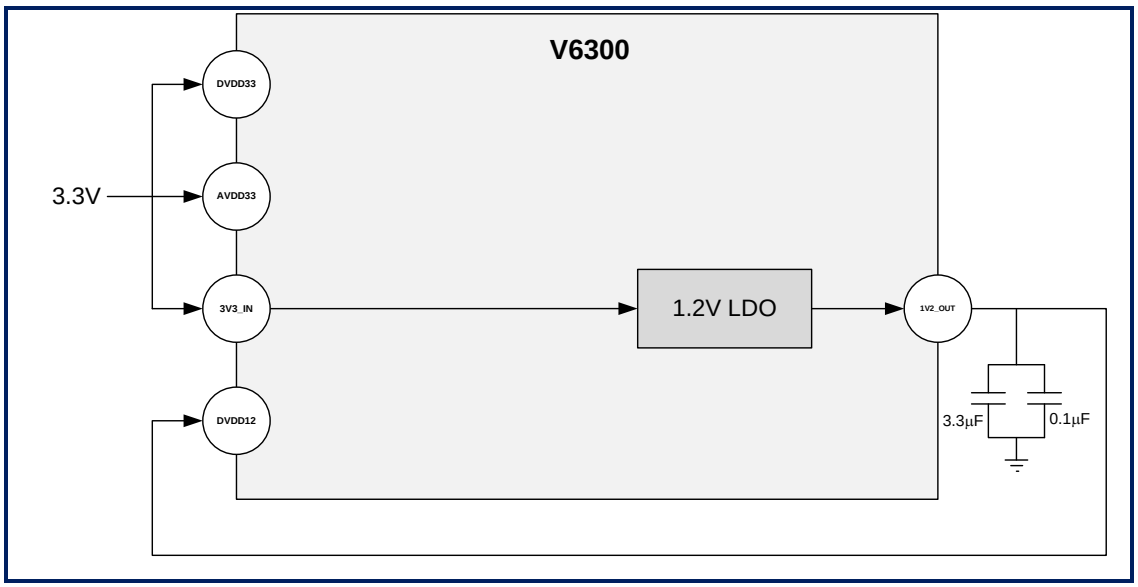


Figure 5-2 Power Supply Architecture

Power on sequence of 3.3V and 1.2V supply voltage is showed in Figure 5-3. It is required if external 1.2V power supply (Other than integrated 3.3V to 1.2V LDO) is used to supply DVDD12. If power supply architecture of Figure 5-4 is used, the power on sequence is guaranteed by the integrated LDO (3.3V to 1.2V).

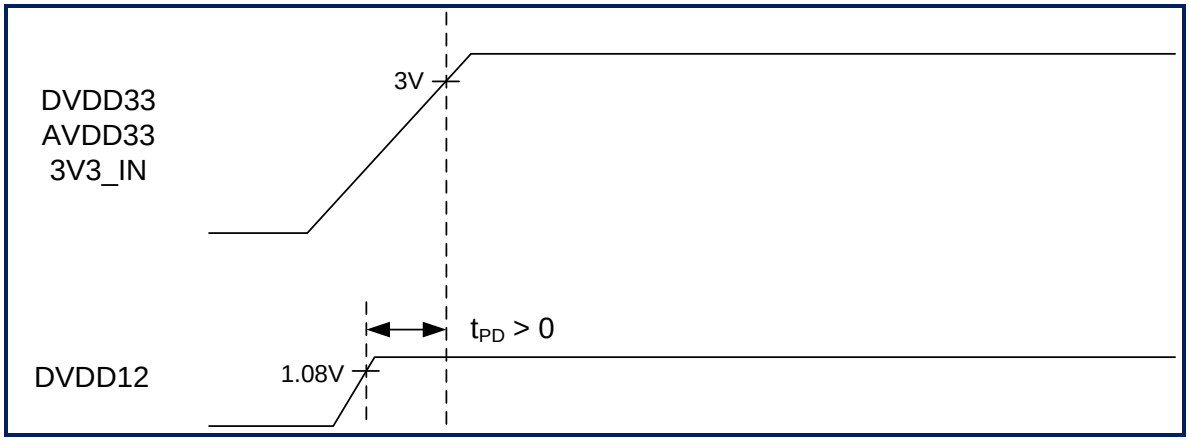
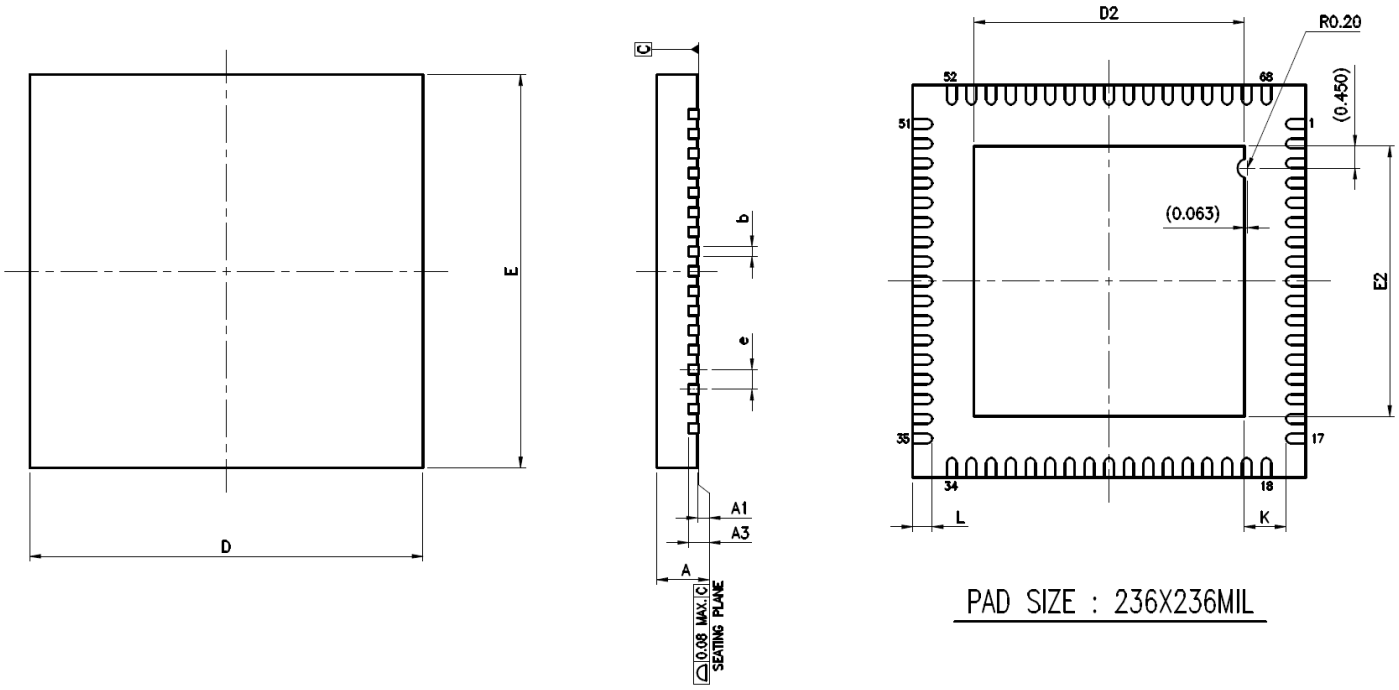


Figure 5-5 Power On Sequence

6. Outline Dimensions

68L-QFN



	PACKAGE TYPE					
JEDEC OUTLINE	MO-220			MO-220		
PKG CODE	WQFN(X868)			VQFN(Y868)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.203 REF.			0.203 REF.		
b	0.15	0.20	0.25	0.15	0.20	0.25
D	8.00 BSC			8.00 BSC		
E	8.00 BSC			8.00 BSC		
e	0.40 BSC			0.40 BSC		
L	0.35	0.40	0.45	0.35	0.40	0.45
K	0.20	—	—	0.20	—	—

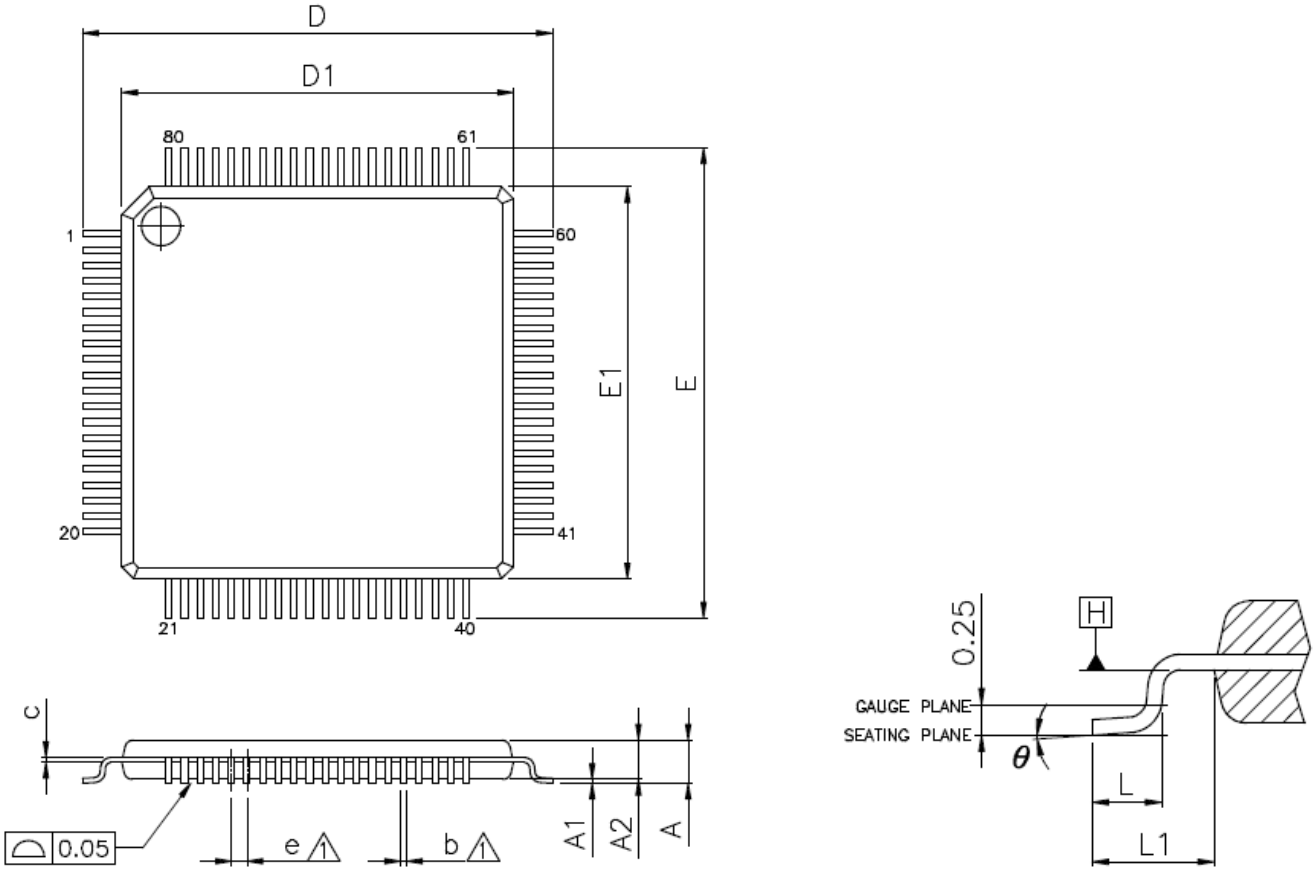
	E2			D2			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
236X236 MIL	5.40	5.50	5.60	5.40	5.50	5.60	V	X	N/A

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 6-1 68L-QFN Package Outline Dimensions

80L-TQFP



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
b	0.13	0.18	0.23
c	0.09	—	0.20
L	0.45	0.60	0.75
L1	1.00 REF		
e	0.40 BSC		
θ	0°	3.5°	7°

NOTES:

1. JEDEC OUTLINE : MS–026 ACE.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

Figure 6-2 80L-TQFP Package Outline Dimensions