

REF19x Series

FEATURES

Initial Accuracy: ± 2 mV Max
Temperature Coefficient: 5 ppm/°C Max
Low Supply Current: 45 μ A Max
Sleep Mode: 15 μ A Max
Low Dropout Voltage
Load Regulation: 4 ppm/mA
Line Regulation: 4 ppm/V
High Output Current: 30 mA
Short-Circuit Protection

APPLICATIONS

Portable Instrumentation
A/D and D/A Converters
Smart Sensors
Solar Powered Applications
Loop Current Powered Instrumentations

GENERAL DESCRIPTION

The REF19x series precision band gap voltage references use a patented temperature drift curvature correction circuit and laser trimming of highly stable thin-film resistors to achieve a very low temperature coefficient and a high initial accuracy.

The REF19x series is made up of micropower, low dropout voltage (LDV) devices providing a stable output voltage from supplies as low as 100 mV above the output voltage and consuming less than 45 μ A of supply current. In sleep mode, which is enabled by applying a low TTL or CMOS level to the **SLEEP** pin, the output is turned off and supply current is further reduced to less than 15 μ A.

The REF19x series references are specified over the extended industrial temperature range (-40°C to $+85^{\circ}\text{C}$) with typical performance specifications over -40°C to $+125^{\circ}\text{C}$ for applications such as automotive.

All electrical grades are available in 8-lead SOIC; the PDIP and TSSOP are available only in the lowest electrical grade. Products are also available in die form.

Test Pins (TP)

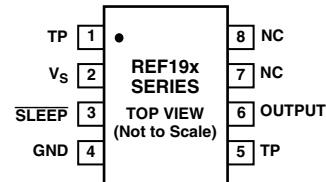
The test pins, Pin 1 and Pin 5, are reserved for in-package Zener-zap. To achieve the highest level of accuracy at the output, the Zener-zapping technique is used to trim the output voltage. Since each unit may require a different amount of adjustment, the resistance value at the test pins will vary widely from pin to pin as well as from part to part. The user should not make any physical or electrical connections to Pin 1 and Pin 5.

REV. F

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

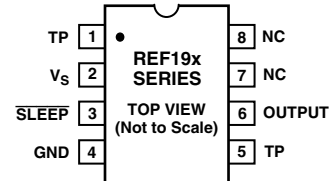
PIN CONFIGURATIONS

8-Lead SOIC and TSSOP
(S Suffix and RU Suffix)



NC = NO CONNECT
TP PINS ARE FACTORY TEST POINTS,
NO USER CONNECTION

8-Lead PDIP (P Suffix)



NC = NO CONNECT
TP PINS ARE FACTORY TEST POINTS,
NO USER CONNECTION

Table I.

| Part Number | Nominal Output Voltage (V) |
|-------------|----------------------------|
| REF191 | 2.048 |
| REF192 | 2.50 |
| REF193 | 3.00 |
| REF194 | 4.50 |
| REF195 | 5.00 |
| REF196 | 3.30 |
| REF198 | 4.096 |

REF19x Series

REF191—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|----------------------------------|--------------------------------|--|-------|-------|----------------------|-------------------|
| INITIAL ACCURACY ¹ | | | | | | |
| E Grade | V_O | $I_{OUT} = 0\text{ mA}$ | 2.046 | 2.048 | 2.050 | V |
| F Grade | | | 2.043 | | 2.053 | V |
| G Grade | | | 2.038 | | 2.058 | V |
| LINE REGULATION ² | | | | | | |
| E Grade | $\Delta V_O / \Delta V_{IN}$ | $3.0\text{ V} \leq V_S \leq 15\text{ V}$, $I_{OUT} = 0\text{ mA}$ | | 2 | 4 | ppm/V |
| F and G Grades | | | | 4 | 8 | ppm/V |
| LOAD REGULATION ² | | | | | | |
| E Grade | $\Delta V_O / \Delta V_{LOAD}$ | $V_S = 5.0\text{ V}$, $0\text{ mA} \leq I_{OUT} \leq 30\text{ mA}$ | | 4 | 10 | ppm/mA |
| F and G Grades | | | | 6 | 15 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S = 3.15\text{ V}$, $I_{LOAD} = 2\text{ mA}$ $V_S = 3.3\text{ V}$, $I_{LOAD} = 10\text{ mA}$ $V_S = 3.6\text{ V}$, $I_{LOAD} = 30\text{ mA}$ | | | 0.95 1.25 1.55 | V V V |
| LONG-TERM STABILITY ³ | DV_O | 1,000 Hours @ 125°C | | 1.2 | | mV |
| NOISE VOLTAGE | ϵ_N | 0.1 Hz to 10 Hz | | 20 | | $\mu\text{V p-p}$ |

NOTES

¹Initial accuracy includes temperature hysteresis effect.

²Line and load regulation specifications include the effect of self-heating.

³Long-term drift is guaranteed by 1,000 hours life test performed on three independent wafer lots at 125°C , with an LTPD of 1.3.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ $V_S = 3.3\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|--------------------------------|--|-----|-----|----------------------|-----------------------|
| TEMPERATURE COEFFICIENT ^{1, 2} | | | | | | |
| E Grade | $TCV_O / ^\circ\text{C}$ | $I_{OUT} = 0\text{ mA}$ | | 2 | 5 | ppm/ $^\circ\text{C}$ |
| F Grade | | | | 5 | 10 | ppm/ $^\circ\text{C}$ |
| G Grade ³ | | | | 10 | 25 | ppm/ $^\circ\text{C}$ |
| LINE REGULATION ⁴ | | | | | | |
| E Grade | $\Delta V_O / \Delta V_{IN}$ | $3.0\text{ V} \leq V_S \leq 15\text{ V}$, $I_{OUT} = 0\text{ mA}$ | | 5 | 10 | ppm/V |
| F and G Grades | | | | 10 | 20 | ppm/V |
| LOAD REGULATION ⁴ | | | | | | |
| E Grade | $\Delta V_O / \Delta V_{LOAD}$ | $V_S = 5.0\text{ V}$, $0\text{ mA} \leq I_{OUT} \leq 25\text{ mA}$ | | 5 | 15 | ppm/mA |
| F and G Grades | | | | 10 | 20 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S = 3.15\text{ V}$, $I_{LOAD} = 2\text{ mA}$ $V_S = 3.3\text{ V}$, $I_{LOAD} = 10\text{ mA}$ $V_S = 3.6\text{ V}$, $I_{LOAD} = 25\text{ mA}$ | | | 0.95 1.25 1.55 | V V V |
| SLEEP PIN | | | | | | |
| Logic High Input Voltage | V_H | | 2.4 | | | V |
| Logic High Input Current | I_H | | | | -8 | μA |
| Logic Low Input Voltage | V_L | | | | 0.8 | V |
| Logic Low Input Current | I_L | | | | -8 | μA |
| SUPPLY CURRENT | | | | | | |
| Sleep Mode | | No Load | | | 45 | μA |
| | | No Load | | | 15 | μA |

NOTES

¹For proper operation, a $1\text{ }\mu\text{F}$ capacitor is required between the output pin and the GND pin of the device.

² TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/ $^\circ\text{C}$.

$$TCV_O = (V_{MAX} - V_{MIN}) / V_O(T_{MAX} - T_{MIN})$$

³Guaranteed by characterization.

⁴Line and load regulation specifications include the effect of self-heating.

Specifications subject to change without notice.

REF191—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = 3.3\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|------------------------------|--|-----|-----|--------------|-----------------------|
| TEMPERATURE COEFFICIENT ^{1, 2} | | | | | | |
| E Grade | $TCV_O/^\circ\text{C}$ | $I_{OUT} = 0\text{ mA}$ | | 2 | | ppm/ $^\circ\text{C}$ |
| F Grade | | | | 5 | | ppm/ $^\circ\text{C}$ |
| G Grade ³ | | | | 10 | | ppm/ $^\circ\text{C}$ |
| LINE REGULATION ⁴ | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{IN}$ | $3.0\text{ V} \leq V_S \leq 15\text{ V}$, $I_{OUT} = 0\text{ mA}$ | | 10 | | ppm/V |
| F and G Grades | | | | 20 | | ppm/V |
| LOAD REGULATION ⁴ | | | | | | |
| E Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S = 5.0\text{ V}$, $0\text{ mA} \leq I_{OUT} \leq 20\text{ mA}$ | | 10 | | ppm/mA |
| F and G Grades | | | | 20 | | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S = 3.3\text{ V}$, $I_{LOAD} = 10\text{ mA}$ $V_S = 3.6\text{ V}$, $I_{LOAD} = 20\text{ mA}$ | | | 1.25 1.55 | V V |

NOTES

¹For proper operation, a 1 μF capacitor is required between the output pin and the GND pin of the device.

² TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/ $^\circ\text{C}$.

$$TCV_O = (V_{MAX} - V_{MIN})/V_O(T_{MAX} - T_{MIN}).$$

³Guaranteed by characterization.

⁴Line and load regulation specifications include the effect of self-heating.

Specifications subject to change without notice.

REF19x Series

REF192—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|----------------------------------|--------------------------------|--|-------|-------|--------------|-------------------|
| INITIAL ACCURACY ¹ | | | | | | |
| E Grade | V_O | $I_{OUT} = 0\text{ mA}$ | 2.498 | 2.500 | 2.502 | V |
| F Grade | | | 2.495 | | 2.505 | V |
| G Grade | | | 2.490 | | 2.510 | V |
| LINE REGULATION ² | | | | | | |
| E Grade | $\Delta V_O / \Delta V_{IN}$ | $3.0\text{ V} \leq V_S \leq 15\text{ V}$, $I_{OUT} = 0\text{ mA}$ | | 2 | 4 | ppm/V |
| F and G Grades | | | | 4 | 8 | ppm/V |
| LOAD REGULATION ² | | | | | | |
| E Grade | $\Delta V_O / \Delta V_{LOAD}$ | $V_S = 5.0\text{ V}$, $0\text{ mA} \leq I_{OUT} \leq 30\text{ mA}$ | | 4 | 10 | ppm/mA |
| F and G Grades | | | | 6 | 15 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S = 3.5\text{ V}$, $I_{LOAD} = 10\text{ mA}$ $V_S = 3.9\text{ V}$, $I_{LOAD} = 30\text{ mA}$ | | | 1.00 1.40 | V V |
| LONG-TERM STABILITY ³ | DV_O | 1,000 Hours @ 125°C | | 1.2 | | mV |
| NOISE VOLTAGE | ϵ_N | 0.1 Hz to 10 Hz | | 25 | | $\mu\text{V p-p}$ |

NOTES

¹Initial accuracy includes temperature hysteresis effect.

²Line and load regulation specifications include the effect of self-heating.

³Long-term drift is guaranteed by 1,000 hours life test performed on three independent wafer lots at 125°C , with an LTPD of 1.3.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ $V_S = 3.3\text{ V}$, $T_A = -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|--------------------------------|--|-----|-----|--------------|--------------------------------|
| TEMPERATURE COEFFICIENT ^{1, 2} | | | | | | |
| E Grade | $TCV_O / ^\circ\text{C}$ | $I_{OUT} = 0\text{ mA}$ | | 2 | 5 | ppm/ $^\circ\text{C}$ |
| F Grade | | | | 5 | 10 | ppm/ $^\circ\text{C}$ |
| G Grade ³ | | | | 10 | 25 | ppm/ $^\circ\text{C}$ |
| LINE REGULATION ⁴ | | | | | | |
| E Grade | $\Delta V_O / \Delta V_{IN}$ | $3.0\text{ V} \leq V_S \leq 15\text{ V}$, $I_{OUT} = 0\text{ mA}$ | | 5 | 10 | ppm/V |
| F and G Grades | | | | 10 | 20 | ppm/V |
| LOAD REGULATION ⁴ | | | | | | |
| E Grade | $\Delta V_O / \Delta V_{LOAD}$ | $V_S = 5.0\text{ V}$, $0\text{ mA} \leq I_{OUT} \leq 25\text{ mA}$ | | 5 | 15 | ppm/mA |
| F and G Grades | | | | 10 | 20 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S = 3.5\text{ V}$, $I_{LOAD} = 10\text{ mA}$ $V_S = 4.0\text{ V}$, $I_{LOAD} = 25\text{ mA}$ | | | 1.00 1.50 | V V |
| SLEEP PIN | | | | | | |
| Logic High Input Voltage | V_H | | 2.4 | | | V |
| Logic High Input Current | I_H | | | | -8 | μA |
| Logic Low Input Voltage | V_L | | | | 0.8 | V |
| Logic Low Input Current | I_L | | | | -8 | μA |
| SUPPLY CURRENT | | | | | | |
| Sleep Mode | | No Load No Load | | | 45 15 | μA μA |

NOTES

¹For proper operation, a $1\text{ }\mu\text{F}$ capacitor is required between the output pin and the GND pin of the device.

² TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/ $^\circ\text{C}$.

$$TCV_O = (V_{MAX} - V_{MIN}) / V_O(T_{MAX} - T_{MIN})$$

³Guaranteed by characterization.

⁴Line and load regulation specifications include the effect of self-heating.

Specifications subject to change without notice.

REF192—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = 3.3\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit | | |
|---|-------------------------------------|--|-----|-----|-----|------|--------|--------|
| TEMPERATURE COEFFICIENT ^{1, 2} | TCV _O /°C | I _{OUT} = 0 mA | | | | | | |
| E Grade | | | | | | | 2 | ppm/°C |
| F Grade | | | | | | | 5 | ppm/°C |
| G Grade ³ | | | | | | 10 | ppm/°C | |
| LINE REGULATION ⁴ | ΔV _O /ΔV _{IN} | 3.0 V ≤ V _S ≤ 15 V, I _{OUT} = 0 mA | | | | | | |
| E Grade | | | | | | | 10 | ppm/V |
| F and G Grades | | | | | | 20 | ppm/V | |
| LOAD REGULATION ⁴ | ΔV _O /ΔV _{LOAD} | V _S = 5.0 V, 0 mA ≤ I _{OUT} ≤ 20 mA | | | | | | |
| E Grade | | | | | | | 10 | ppm/mA |
| F and G Grades | | | | | | 20 | ppm/mA | |
| DROPOUT VOLTAGE | V _S - V _O | V _S = 3.5 V, I _{LOAD} = 10 mA V _S = 4.0 V, I _{LOAD} = 20 mA | | | | | 1.00 | V |
| | | | | | | | 1.50 | V |

NOTES

¹For proper operation, a 1 μF capacitor is required between the output pin and the GND pin of the device.

²TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.

$$TCV_O = (V_{MAX} - V_{MIN}) / V_O(T_{MAX} - T_{MIN})$$

³Guaranteed by characterization.

⁴Line and load regulation specifications include the effect of self-heating.

Specifications subject to change without notice.

REF193—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit | | |
|----------------------------------|-------------------------------------|--|-------|-----|-------|--------|------|----|
| INITIAL ACCURACY ¹ | V _O | I _{OUT} = 0 mA | 2.990 | 3.0 | 3.010 | V | | |
| G Grade | | | | | | | | |
| LINE REGULATION ² | ΔV _O /ΔV _{IN} | 3.3 V, ≤ V _S ≤ 15 V, I _{OUT} = 0 mA | | | | | | |
| G Grades | | | | | | | 4 | 8 |
| LOAD REGULATION ² | ΔV _O /ΔV _{LOAD} | V _S = 5.0 V, 0 mA ≤ I _{OUT} ≤ 30 mA | | | | | | |
| G Grade | | | | | | | 6 | 15 |
| DROPOUT VOLTAGE | V _S - V _O | V _S = 3.8 V, I _{LOAD} = 10 mA V _S = 4.0 V, I _{LOAD} = 30 mA | | | | | 0.80 | V |
| | | | | | | | 1.00 | V |
| LONG-TERM STABILITY ³ | DV _O | 1,000 Hours @ 125°C | | 1.2 | | mV | | |
| NOISE VOLTAGE | e _N | 0.1 Hz to 10 Hz | | 30 | | μV p-p | | |

NOTES

¹Initial accuracy includes temperature hysteresis effect.

²Line and load regulation specifications include the effect of self-heating.

³Long-term drift is guaranteed by 1,000 hours life test performed on three independent wafer lots at 125°C, with an LTPD of 1.3.

Specifications subject to change without notice.

REF19x Series

REF193—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = 3.3\text{ V}$, $T_A = -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|------------------------------|---|---------|-----|------|-----------------------|
| TEMPERATURE COEFFICIENT ^{1, 2} G Grade ³ | $TCV_O/^\circ\text{C}$ | $I_{OUT} = 0\text{ mA}$ | | 10 | 25 | ppm/ $^\circ\text{C}$ |
| LINE REGULATION ⁴ G Grade | $\Delta V_O/\Delta V_{IN}$ | $3.3\text{ V} \leq V_S \leq 15\text{ V}$, $I_{OUT} = 0\text{ mA}$ | | 10 | 20 | ppm/V |
| LOAD REGULATION ⁴ G Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S = 5.0\text{ V}$, $0\text{ mA} \leq I_{OUT} \leq 25\text{ mA}$ | | 10 | 20 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S = 3.8\text{ V}$, $I_{LOAD} = 10\text{ mA}$ | | | 0.80 | V |
| | | $V_S = 4.1\text{ V}$, $I_{LOAD} = 30\text{ mA}$ | | | 1.10 | V |
| SLEEP PIN | | | 2.4 | | | |
| Logic High Input Voltage | V_H | | | | | V |
| Logic High Input Current | I_H | | | | -8 | μA |
| Logic Low Input Voltage | V_L | | | | 0.8 | V |
| Logic Low Input Current | I_L | | | | -8 | μA |
| SUPPLY CURRENT | | No Load | | | 45 | μA |
| | | Sleep Mode | No Load | | 15 | μA |

NOTES

¹For proper operation, a 1 μF capacitor is required between the output pin and the GND pin of the device.

² TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/ $^\circ\text{C}$.

$$TCV_O = (V_{MAX} - V_{MIN}) / V_O(T_{MAX} - T_{MIN}).$$

³Guaranteed by characterization.

⁴Line and load regulation specifications include the effect of self-heating.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ $V_S = 3.3\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|------------------------------|---|-----|-----|------|-----------------------|
| TEMPERATURE COEFFICIENT ^{1, 2} G Grade ³ | $TCV_O/^\circ\text{C}$ | $I_{OUT} = 0\text{ mA}$ | | 10 | | ppm/ $^\circ\text{C}$ |
| LINE REGULATION ⁴ G Grade | $\Delta V_O/\Delta V_{IN}$ | $3.3\text{ V} \leq V_S \leq 15\text{ V}$, $I_{OUT} = 0\text{ mA}$ | | 20 | | ppm/V |
| LOAD REGULATION ⁴ G Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S = 5.0\text{ V}$, $0\text{ mA} \leq I_{OUT} \leq 20\text{ mA}$ | | 10 | | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S = 3.8\text{ V}$, $I_{LOAD} = 10\text{ mA}$ | | | 0.80 | V |
| | | $V_S = 4.1\text{ V}$, $I_{LOAD} = 20\text{ mA}$ | | | 1.10 | V |

NOTES

¹For proper operation, a 1 μF capacitor is required between the output pin and the GND pin of the device.

² TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/ $^\circ\text{C}$.

$$TCV_O = (V_{MAX} - V_{MIN}) / V_O(T_{MAX} - T_{MIN}).$$

³Guaranteed by characterization.

⁴Line and load regulation specifications include the effect of self-heating.

Specifications subject to change without notice.

REF194—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|----------------------------------|--------------------------------|---|-------|-----|-------|-------------------|
| INITIAL ACCURACY ¹ | | | | | | |
| E Grade | V_O | $I_{OUT} = 0\text{ mA}$ | 4.498 | 4.5 | 4.502 | V |
| F Grade | | | 4.495 | | 4.505 | V |
| G Grade | | | 4.490 | | 4.510 | V |
| LINE REGULATION ² | | | | | | |
| E Grade | $\Delta V_O / \Delta V_{IN}$ | $4.75\text{ V} \leq V_S \leq 15\text{ V}$, $I_{OUT} = 0\text{ mA}$ | | 2 | 4 | ppm/V |
| F and G Grades | | | | 4 | 8 | ppm/V |
| LOAD REGULATION ² | | | | | | |
| E Grade | $\Delta V_O / \Delta V_{LOAD}$ | $V_S = 5.8\text{ V}$, $0\text{ mA} \leq I_{OUT} \leq 30\text{ mA}$ | | 2 | 4 | ppm/mA |
| F and G Grades | | | | 4 | 8 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S = 5.00\text{ V}$, $I_{LOAD} = 10\text{ mA}$ $V_S = 5.8\text{ V}$, $I_{LOAD} = 30\text{ mA}$ | | | 0.50 | V |
| | | | | | | 1.30 |
| LONG-TERM STABILITY ³ | DV_O | 1,000 Hours @ 125°C | | 2 | | mV |
| NOISE VOLTAGE | e_N | 0.1 Hz to 10 Hz | | 45 | | $\mu\text{V p-p}$ |

NOTES

¹Initial accuracy includes temperature hysteresis effect.

²Line and load regulation specifications include the effect of self-heating.

³Long-term drift is guaranteed by 1,000 hours life test performed on three independent wafer lots at 125°C , with an LTPD of 1.3.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ $V_S = 5.0\text{ V}$, $T_A = -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|--------------------------------|--|-----|-----|----------|--------------------------------|
| TEMPERATURE COEFFICIENT ^{1, 2} | | | | | | |
| E Grade | $TCV_O / ^\circ\text{C}$ | $I_{OUT} = 0\text{ mA}$ | | 2 | 5 | ppm/ $^\circ\text{C}$ |
| F Grade | | | | 5 | 10 | ppm/ $^\circ\text{C}$ |
| G Grade ³ | | | | 10 | 25 | ppm/ $^\circ\text{C}$ |
| LINE REGULATION ⁴ | | | | | | |
| E Grade | $\Delta V_O / \Delta V_{IN}$ | $4.75\text{ V} \leq V_S \leq 15\text{ V}$, $I_{OUT} = 0\text{ mA}$ | | 5 | 10 | ppm/V |
| F and G Grades | | | | 10 | 20 | ppm/V |
| LOAD REGULATION ⁴ | | | | | | |
| E Grade | $\Delta V_O / \Delta V_{LOAD}$ | $V_S = 5.80\text{ V}$, $0\text{ mA} \leq I_{OUT} \leq 25\text{ mA}$ | | 5 | 15 | ppm/mA |
| F and G Grades | | | | 10 | 20 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S = 5.00\text{ V}$, $I_{LOAD} = 10\text{ mA}$ $V_S = 5.80\text{ V}$, $I_{LOAD} = 25\text{ mA}$ | | | 0.5 | V |
| | | | | | | 1.30 |
| SLEEP PIN | | | | | | |
| Logic High Input Voltage | V_H | | 2.4 | | | V |
| Logic High Input Current | I_H | | | | -8 | μA |
| Logic Low Input Voltage | V_L | | | | 0.8 | V |
| Logic Low Input Current | I_L | | | | -8 | μA |
| SUPPLY CURRENT | | | | | | |
| Sleep Mode | | No Load No Load | | | 45 15 | μA μA |

NOTES

¹For proper operation, a $1\text{ }\mu\text{F}$ capacitor is required between the output pin and the GND pin of the device.

² TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/ $^\circ\text{C}$.

$$TCV_O = (V_{MAX} - V_{MIN}) / V_O(T_{MAX} - T_{MIN}).$$

³Guaranteed by characterization.

⁴Line and load regulation specifications include the effect of self-heating.

Specifications subject to change without notice.

REF19x Series

REF194—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = 5.0\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit | | |
|---|---------------------------------|--|-----|-----|------|------|---|--------|
| TEMPERATURE COEFFICIENT ^{1, 2} | TCV _O /°C | I _{OUT} = 0 mA | | | | | | |
| E Grade | | | | | | | 2 | ppm/°C |
| F Grade | | | | | | | 5 | ppm/°C |
| G Grade ³ | 10 | ppm/°C | | | | | | |
| LINE REGULATION ⁴ | $\Delta V_O / \Delta V_{IN}$ | 4.75 V ≤ V _S ≤ 15 V, I _{OUT} = 0 mA | | | | | | |
| E Grade | | | | | | | 5 | ppm/V |
| F and G Grades | 10 | ppm/V | | | | | | |
| LOAD REGULATION ⁴ | $\Delta V_O / \Delta V_{LOAD}$ | V _S = 5.80 V, mA 0 ≤ I _{OUT} ≤ 20 mA | | | | | | |
| E Grade | | | | | | | 5 | ppm/mA |
| F and G Grades | 10 | ppm/mA | | | | | | |
| DROPOUT VOLTAGE | V _S - V _O | V _S = 5.10 V, I _{LOAD} = 10 mA | | | 0.60 | V | | |
| | | V _S = 5.95 V, I _{LOAD} = 20 mA | | | 1.45 | V | | |

NOTES

¹For proper operation, a 1 μF capacitor is required between the output pin and the GND pin of the device.

²TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.

$$TCV_O = (V_{MAX} - V_{MIN}) / V_O (T_{MAX} - T_{MIN})$$

³Guaranteed by characterization.

⁴Line and load regulation specifications include the effect of self-heating.

Specifications subject to change without notice.

REF195—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = 5.10\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|----------------------------------|--------------------------------|--|-------|-----|--------------|-------------------|
| INITIAL ACCURACY ¹ | | | | | | |
| E Grade | V_O | $I_{OUT} = 0\text{ mA}$ | 4.998 | 5.0 | 5.002 | V |
| F Grade | | | 4.995 | | 5.005 | V |
| G Grade | | | 4.990 | | 5.010 | V |
| LINE REGULATION ² | | | | | | |
| E Grade | $\Delta V_O / \Delta V_{IN}$ | $5.10\text{ V} \leq V_S \leq 15\text{ V}$, $I_{OUT} = 0\text{ mA}$ | | 2 | 4 | ppm/V |
| F and G Grades | | | | 4 | 8 | ppm/V |
| LOAD REGULATION ² | | | | | | |
| E Grade | $\Delta V_O / \Delta V_{LOAD}$ | $V_S = 6.30\text{ V}$, $0\text{ mA} \leq I_{OUT} \leq 30\text{ mA}$ | | 2 | 4 | ppm/mA |
| F and G Grades | | | | 4 | 8 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S = 5.50\text{ V}$, $I_{LOAD} = 10\text{ mA}$ $V_S = 6.30\text{ V}$, $I_{LOAD} = 30\text{ mA}$ | | | 0.50 1.30 | V V |
| LONG-TERM STABILITY ³ | DV_O | 1,000 Hours @ 125°C | | 1.2 | | mV |
| NOISE VOLTAGE | e_N | 0.1 Hz to 10 Hz | | 50 | | $\mu\text{V p-p}$ |

NOTES

¹Initial accuracy includes temperature hysteresis effect.

²Line and load regulation specifications include the effect of self-heating.

³Long-term drift is guaranteed by 1,000 hours life test performed on three independent wafer lots at 125°C , with an LTPD of 1.3.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ $V_S = 5.15\text{ V}$, $T_A = -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|--------------------------------|--|-----|-----|--------------|--------------------------------|
| TEMPERATURE COEFFICIENT ^{1, 2} | | | | | | |
| E Grade | $TCV_O / ^\circ\text{C}$ | $I_{OUT} = 0\text{ mA}$ | | 2 | 5 | ppm/ $^\circ\text{C}$ |
| F Grade | | | | 5 | 10 | ppm/ $^\circ\text{C}$ |
| G Grade ³ | | | | 10 | 25 | ppm/ $^\circ\text{C}$ |
| LINE REGULATION ⁴ | | | | | | |
| E Grade | $\Delta V_O / \Delta V_{IN}$ | $5.15\text{ V} \leq V_S \leq 15\text{ V}$, $I_{OUT} = 0\text{ mA}$ | | 5 | 10 | ppm/V |
| F and G Grades | | | | 10 | 20 | ppm/V |
| LOAD REGULATION ⁴ | | | | | | |
| E Grade | $\Delta V_O / \Delta V_{LOAD}$ | $V_S = 6.30\text{ V}$, $0\text{ mA} \leq I_{OUT} \leq 25\text{ mA}$ | | 5 | 10 | ppm/mA |
| F and G Grades | | | | 10 | 20 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S = 5.50\text{ V}$, $I_{LOAD} = 10\text{ mA}$ $V_S = 6.30\text{ V}$, $I_{LOAD} = 25\text{ mA}$ | | | 0.50 1.30 | V V |
| SLEEP PIN | | | | | | |
| Logic High Input Voltage | V_H | | 2.4 | | | V |
| Logic High Input Current | I_H | | | | -8 | μA |
| Logic Low Input Voltage | V_L | | | | 0.8 | V |
| Logic Low Input Current | I_L | | | | -8 | μA |
| SUPPLY CURRENT | | | | | | |
| Sleep Mode | | No Load No Load | | | 45 15 | μA μA |

NOTES

¹For proper operation, a 1 μF capacitor is required between the output pin and the GND pin of the device.

² TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/ $^\circ\text{C}$.

$$TCV_O = (V_{MAX} - V_{MIN}) / V_O(T_{MAX} - T_{MIN})$$

³Guaranteed by characterization.

⁴Line and load regulation specifications include the effect of self-heating.

Specifications subject to change without notice.

REF19x Series

REF195—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = 5.20\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit | | |
|---|-------------------------------------|--|-----|-----|-----|------|--------|--------|
| TEMPERATURE COEFFICIENT ^{1, 2} | TCV _O /°C | I _{OUT} = 0 mA | | | | | | |
| E Grade | | | | | | | 2 | ppm/°C |
| F Grade | | | | | | | 5 | ppm/°C |
| G Grade ³ | | | | | | 10 | ppm/°C | |
| LINE REGULATION ⁴ | ΔV _O /ΔV _{IN} | 5.20 V ≤ V _S ≤ 15 V, I _{OUT} = 0 mA | | | | | | |
| E Grade | | | | | | | 5 | ppm/V |
| F and G Grades | | | | | | 10 | ppm/V | |
| LOAD REGULATION ⁴ | ΔV _O /ΔV _{LOAD} | V _S = 6.45 V, 0 mA ≤ I _{OUT} ≤ 20 mA | | | | | | |
| E Grade | | | | | | | 5 | ppm/mA |
| F and G Grades | | | | | | 10 | ppm/mA | |
| DROPOUT VOLTAGE | V _S - V _O | V _S = 5.60 V, I _{LOAD} = 10 mA | | | | 0.60 | V | |
| | | V _S = 6.45 V, I _{LOAD} = 20 mA | | | | 1.45 | V | |

NOTES

¹For proper operation, a 1 μF capacitor is required between the output pin and the GND pin of the device.

²TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.

$$TCV_O = (V_{MAX} - V_{MIN}) / V_O(T_{MAX} - T_{MIN})$$

³Guaranteed by characterization.

⁴Line and load regulation specifications include the effect of self-heating.

Specifications subject to change without notice.

REF196—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = 3.5\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit | |
|----------------------------------|-------------------------------------|---|-------|-----|-------|--------|---|
| INITIAL ACCURACY ¹ | V _O | I _{OUT} = 0 mA | 3.290 | 3.3 | 3.310 | V | |
| G Grade | | | | | | | |
| LINE REGULATION ² | ΔV _O /ΔV _{IN} | 3.50 V ≤ V _S ≤ 15 V, I _{OUT} = 0 mA | | | | | |
| G Grades | | | | | | | 4 |
| LOAD REGULATION ² | ΔV _O /ΔV _{LOAD} | V _S = 5.0 V, 0 mA ≤ I _{OUT} ≤ 30 mA | | | | | |
| G Grade | | | | | | | 6 |
| DROPOUT VOLTAGE | V _S - V _O | V _S = 4.1 V, I _{LOAD} = 10 mA | | | | 0.80 | V |
| | | V _S = 4.3 V, I _{LOAD} = 30 mA | | | | 1.00 | V |
| LONG-TERM STABILITY ³ | DV _O | 1,000 Hours @ 125°C | | 1.2 | | mV | |
| NOISE VOLTAGE | e _N | 0.1 Hz to 10 Hz | | 33 | | μV p-p | |

NOTES

¹Initial accuracy includes temperature hysteresis effect.

²Line and load regulation specifications include the effect of self-heating.

³Long-term drift is guaranteed by 1,000 hours life test performed on three independent wafer lots at 125°C, with an LTPD of 1.3.

Specifications subject to change without notice.

REF196—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = 3.5\text{ V}$, $T_A = -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|------------------------------|---|-----|-----|------|-----------------------|
| TEMPERATURE COEFFICIENT ^{1, 2} G Grade ³ | $TCV_O/^\circ\text{C}$ | $I_{OUT} = 0\text{ mA}$ | | 10 | 25 | ppm/ $^\circ\text{C}$ |
| LINE REGULATION ⁴ G Grade | $\Delta V_O/\Delta V_{IN}$ | $3.5\text{ V} \leq V_S \leq 15\text{ V}$, $I_{OUT} = 0\text{ mA}$ | | 10 | 20 | ppm/V |
| LOAD REGULATION ⁴ G Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S = 5.0\text{ V}$, $0\text{ mA} \leq I_{OUT} \leq 25\text{ mA}$ | | 10 | 20 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S = 4.1\text{ V}$, $I_{LOAD} = 10\text{ mA}$ | | | 0.80 | V |
| | | $V_S = 4.3\text{ V}$, $I_{LOAD} = 25\text{ mA}$ | | | 1.00 | V |
| SLEEP PIN | | | | | | |
| Logic High Input Voltage | V_H | | 2.4 | | | V |
| Logic High Input Current | I_H | | | | -8 | μA |
| Logic Low Input Voltage | V_L | | | | 0.8 | V |
| Logic Low Input Current | I_L | | | | -8 | μA |
| SUPPLY CURRENT | | | | | | |
| Sleep Mode | | No Load | | | 45 | μA |
| | | No Load | | | 15 | μA |

NOTES

¹For proper operation, a 1 μF capacitor is required between the output pin and the GND pin of the device.

² TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/ $^\circ\text{C}$.

$$TCV_O = (V_{MAX} - V_{MIN}) / V_O(T_{MAX} - T_{MIN}).$$

³Guaranteed by characterization.

⁴Line and load regulation specifications include the effect of self-heating.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ $V_S = 3.50\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|------------------------------|---|-----|-----|------|-----------------------|
| TEMPERATURE COEFFICIENT ^{1, 2} G Grade ³ | $TCV_O/^\circ\text{C}$ | $I_{OUT} = 0\text{ mA}$ | | 10 | | ppm/ $^\circ\text{C}$ |
| LINE REGULATION ⁴ G Grade | $\Delta V_O/\Delta V_{IN}$ | $3.50\text{ V} \leq V_S \leq 15\text{ V}$, $I_{OUT} = 0\text{ mA}$ | | 20 | | ppm/V |
| LOAD REGULATION ⁴ G Grade | $\Delta V_O/\Delta V_{LOAD}$ | $V_S = 5.0\text{ V}$, $0\text{ mA} \leq I_{OUT} \leq 20\text{ mA}$ | | 20 | | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S = 4.1\text{ V}$, $I_{LOAD} = 10\text{ mA}$ | | | 0.80 | V |
| | | $V_S = 4.4\text{ V}$, $I_{LOAD} = 20\text{ mA}$ | | | 1.10 | V |

NOTES

¹For proper operation, a 1 μF capacitor is required between the output pin and the GND pin of the device.

² TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/ $^\circ\text{C}$.

$$TCV_O = (V_{MAX} - V_{MIN}) / V_O(T_{MAX} - T_{MIN}).$$

³Guaranteed by characterization.

⁴Line and load regulation specifications include the effect of self-heating.

Specifications subject to change without notice.

REF19x Series

REF198—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|----------------------------------|--------------------------------|--|-------|-------|--------------|-------------------|
| INITIAL ACCURACY ¹ | | | | | | |
| E Grade | V_O | $I_{OUT} = 0\text{ mA}$ | 4.094 | 4.096 | 4.098 | V |
| F Grade | | | 4.091 | | 4.101 | V |
| G Grade | | | 4.086 | | 4.106 | V |
| LINE REGULATION ² | | | | | | |
| E Grade | $\Delta V_O / \Delta V_{IN}$ | $4.5\text{ V} \leq V_S \leq 15\text{ V}$, $I_{OUT} = 0\text{ mA}$ | | 2 | 4 | ppm/V |
| F and G Grades | | | | 4 | 8 | ppm/V |
| LOAD REGULATION ² | | | | | | |
| E Grade | $\Delta V_O / \Delta V_{LOAD}$ | $V_S = 5.4\text{ V}$, $0\text{ mA} \leq I_{OUT} \leq 30\text{ mA}$ | | 2 | 4 | ppm/mA |
| F and G Grades | | | | 4 | 8 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S = 4.6\text{ V}$, $I_{LOAD} = 10\text{ mA}$ $V_S = 5.4\text{ V}$, $I_{LOAD} = 30\text{ mA}$ | | | 0.50 1.30 | V V |
| LONG-TERM STABILITY ³ | DV_O | 1,000 Hours @ 125°C | | 1.2 | | mV |
| NOISE VOLTAGE | ϵ_N | 0.1 Hz to 10 Hz | | 40 | | $\mu\text{V p-p}$ |

NOTES

¹Initial accuracy includes temperature hysteresis effect.

²Line and load regulation specifications include the effect of self-heating.

³Long-term drift is guaranteed by 1,000 hours life test performed on three independent wafer lots at 125°C , with an LTPD of 1.3.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ $V_S = 5.0\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|--------------------------------|--|-----|-----|--------------|--------------------------------|
| TEMPERATURE COEFFICIENT ^{1, 2} | | | | | | |
| E Grade | $TCV_O / ^\circ\text{C}$ | $I_{OUT} = 0\text{ mA}$ | | 2 | 5 | ppm/ $^\circ\text{C}$ |
| F Grade | | | | 5 | 10 | ppm/ $^\circ\text{C}$ |
| G Grade ³ | | | | 10 | 25 | ppm/ $^\circ\text{C}$ |
| LINE REGULATION ⁴ | | | | | | |
| E Grade | $\Delta V_O / \Delta V_{IN}$ | $4.5\text{ V} \leq V_S \leq 15\text{ V}$, $I_{OUT} = 0\text{ mA}$ | | 5 | 10 | ppm/V |
| F and G Grades | | | | 10 | 20 | ppm/V |
| LOAD REGULATION ⁴ | | | | | | |
| E Grade | $\Delta V_O / \Delta V_{LOAD}$ | $V_S = 5.4\text{ V}$, $0\text{ mA} \leq I_{OUT} \leq 25\text{ mA}$ | | 5 | 10 | ppm/mA |
| F and G Grades | | | | 10 | 20 | ppm/mA |
| DROPOUT VOLTAGE | $V_S - V_O$ | $V_S = 4.6\text{ V}$, $I_{LOAD} = 10\text{ mA}$ $V_S = 5.4\text{ V}$, $I_{LOAD} = 25\text{ mA}$ | | | 0.50 1.30 | V V |
| SLEEP PIN | | | | | | |
| Logic High Input Voltage | V_H | | 2.4 | | | V |
| Logic High Input Current | I_H | | | | -8 | μA |
| Logic Low Input Voltage | V_L | | | | 0.8 | V |
| Logic Low Input Current | I_L | | | | -8 | μA |
| SUPPLY CURRENT | | | | | | |
| Sleep Mode | | No Load No Load | | | 45 15 | μA μA |

NOTES

¹For proper operation, a $1\text{ }\mu\text{F}$ capacitor is required between the output pin and the GND pin of the device.

² TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/ $^\circ\text{C}$.

$$TCV_O = (V_{MAX} - V_{MIN}) / V_O(T_{MAX} - T_{MIN})$$

³Guaranteed by characterization.

⁴Line and load regulation specifications include the effect of self-heating.

Specifications subject to change without notice.

REF198—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = 5.0\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted.)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit | | |
|---|---------------------------------|---|-----|-----|-----|------|---|--------|
| TEMPERATURE COEFFICIENT ^{1, 2} | TCV _O /°C | I _{OUT} = 0 mA | | | | | | |
| E Grade | | | | | | | 2 | ppm/°C |
| F Grade | | | | | | | 5 | ppm/°C |
| G Grade ³ | | | | | | 10 | ppm/°C | |
| LINE REGULATION ⁴ | $\Delta V_O / \Delta V_{IN}$ | 4.5 V ≤ V _S ≤ 15 V, I _{OUT} = 0 mA | | | | | | |
| E Grade | | | | | | | 5 | ppm/V |
| F and G Grades | | | | | | 10 | ppm/V | |
| LOAD REGULATION ⁴ | $\Delta V_O / \Delta V_{LOAD}$ | V _S = 5.6 V, 0 mA ≤ I _{OUT} ≤ 20 mA | | | | | | |
| E Grade | | | | | | | 5 | ppm/mA |
| F and G Grades | | | | | | 10 | ppm/mA | |
| DROPOUT VOLTAGE | V _S - V _O | V _S = 4.7 V, I _{LOAD} = 10 mA | | | | | | |
| | | | | | | | V _S = 5.6 V, I _{LOAD} = 20 mA | 0.60 |
| | | | | | | 1.50 | V | |

NOTES

¹For proper operation, a 1 μF capacitor is required between the output pin and the GND pin of the device.

²TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.

$$TCV_O = (V_{MAX} - V_{MIN}) / V_O (T_{MAX} - T_{MIN})$$

³Guaranteed by characterization.

⁴Line and load regulation specifications include the effect of self-heating.

Specifications subject to change without notice.

WAFER TEST LIMITS (@ I_{LOAD} = 0 mA, T_A = 25°C, unless otherwise noted.)

| Parameter | Symbol | Condition | Limit | Unit | | |
|------------------|------------------------------------|--|-------|--------|---------------------------|------|
| INITIAL ACCURACY | V _O | | | | | |
| REF191 | | | | | 2.043/2.053 | V |
| REF192 | | | | | 2.495/2.505 | V |
| REF193 | | | | | 2.990/3.010 | V |
| REF194 | | | | | 4.495/4.505 | V |
| REF195 | | | | | 4.995/5.005 | V |
| REF196 | | | | | 3.290/3.310 | V |
| REF198 | 4.091/4.101 | V | | | | |
| LINE REGULATION | $\Delta V_O / \Delta V_{IN}$ | (V _O + 0.5 V) < V _{IN} < 15 V, I _{OUT} = 0 mA | 15 | ppm/V | | |
| LOAD REGULATION | $\Delta V_O / \Delta I_{LOAD}$ | 0 mA < I _{LOAD} < 30 mA, V _{IN} = (V _O + 1.3 V) | 15 | ppm/mA | | |
| DROPOUT VOLTAGE | V _O - V+ | I _{LOAD} = 10 mA | | | | |
| | | | | | I _{LOAD} = 30 mA | 1.25 |
| | | | | | 1.55 | V |
| SLEEP MODE INPUT | V _{IH} V _{IL} | | | | | |
| Logic Input High | | | | | 2.4 | V |
| Logic Input Low | | | | | 0.8 | V |
| SUPPLY CURRENT | V _{IN} = 15 V | No Load | | | | |
| | | | | | Sleep Mode | 45 |
| | | No Load | | | 15 | μA |

For proper operation, a 1 μF capacitor is required between the output pins and the GND pin of the REF19x. Electrical tests and wafer probe to the limits shown.

Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

REF19x Series

ABSOLUTE MAXIMUM RATINGS^{1,2}

| | |
|---|-----------------------|
| Supply Voltage | -0.3 V, +18 V |
| Output to GND | -0.3 V, $V_S + 0.3$ V |
| Output to GND Short-Circuit Duration | Indefinite |
| Storage Temperature Range | |
| P, S Package | -65°C to +150°C |
| Operating Temperature Range | |
| REF19x | -40°C to +85°C |
| Junction Temperature Range | |
| P, S Package | -65°C to +150°C |
| Lead Temperature Range (Soldering 60 sec) | 300°C |

| Package Type | θ_{JA} ³ | θ_{JC} | Unit |
|-------------------|----------------------------|---------------|------|
| 8-Lead PDIP (P) | 103 | 43 | °C/W |
| 8-Lead SOIC (S) | 158 | 43 | °C/W |
| 8-Lead TSSOP (RU) | 240 | 43 | °C/W |

NOTES

¹ Absolute maximum rating applies to both DICE and packaged parts, unless otherwise noted.

² Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

³ θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for device in socket for PDIP, and θ_{JA} is specified for device soldered in circuit board for SOIC package.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the REF19x features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ORDERING GUIDE

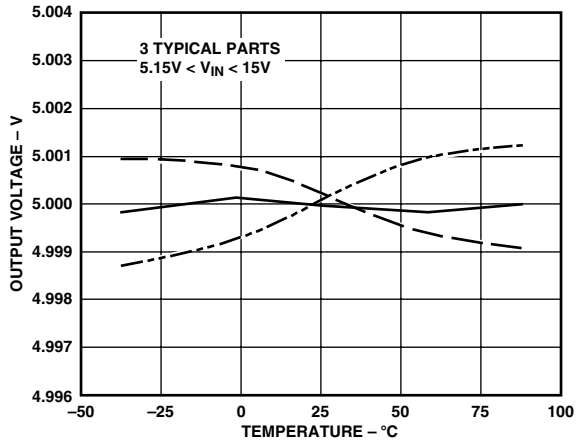
| Model | Temperature Range | Package Description | Package Option | Minimum Quantities/ Reel |
|------------------|-------------------|---------------------|----------------|--------------------------|
| REF191ES | -40°C to +85°C | 8-Lead SOIC | R-8 | 2,500 |
| REF191ES-REEL | -40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF191GP | -40°C to +85°C | 8-Lead PDIP | N-8 | |
| REF191GS | -40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF191GS-REEL7 | -40°C to +85°C | 8-Lead SOIC | R-8 | 1,000 |
| REF192ES | -40°C to +85°C | 8-Lead SOIC | R-8 | 2,500 |
| REF192ES-REEL | -40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF192ES-REEL7 | -40°C to +85°C | 8-Lead SOIC | R-8 | 1,000 |
| REF192FS | -40°C to +85°C | 8-Lead SOIC | R-8 | 2,500 |
| REF192FS-REEL | -40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF192FS-REEL7 | -40°C to +85°C | 8-Lead SOIC | R-8 | 1,000 |
| REF192FSZ-REEL7* | -40°C to +85°C | 8-Lead SOIC | R-8 | 1,000 |
| REF192GP | -40°C to +85°C | 8-Lead PDIP | N-8 | 1,000 |
| REF192GRU | -40°C to +85°C | 8-Lead TSSOP | RU-8 | |
| REF192GRU-REEL7 | -40°C to +85°C | 8-Lead TSSOP | RU-8 | 1,000 |
| REF192GS | -40°C to +85°C | 8-Lead SOIC | R-8 | 2,500 |
| REF192GS-REEL | -40°C to +85°C | 8-Lead SOIC | R-8 | |
| REF192GS-REEL7 | -40°C to +85°C | 8-Lead SOIC | R-8 | 1,000 |
| REF192GSZ-REEL7* | -40°C to +85°C | 8-Lead SOIC | R-8 | 1,000 |

ORDERING GUIDE (continued)

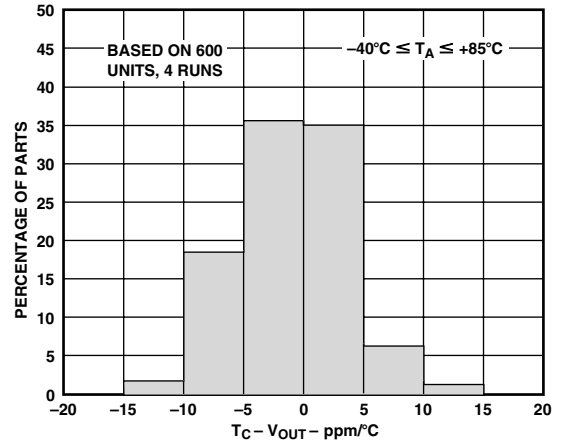
| Model | Temperature Range | Package Description | Package Option | Minimum Quantities/ Reel |
|---|--|---|---|--|
| REF193GS REF193GS-REEL | -40°C to +85°C -40°C to +85°C | 8-Lead SOIC 8-Lead SOIC | R-8 R-8 | 2,500 |
| REF194ES REF194ES-REEL REF194FS REF194GP REF194GS REF194GS-REEL REF194GS-REEL7 | -40°C to +85°C -40°C to +85°C -40°C to +85°C -40°C to +85°C -40°C to +85°C -40°C to +85°C -40°C to +85°C | 8-Lead SOIC 8-Lead SOIC 8-Lead SOIC 8-Lead PDIP 8-Lead SOIC 8-Lead SOIC 8-Lead SOIC | R-8 R-8 R-8 N-8 R-8 R-8 R-8 | 2,500 2,500 2,500 1,000 |
| REF195ES REF195ES-REEL REF195FS REF195FS-REEL REF195GP REF195GRU REF195GRU-REEL7 REF195GS REF195GS-REEL REF195GS-REEL7 REF195GSZ-REEL7* | -40°C to +85°C -40°C to +85°C -40°C to +85°C -40°C to +85°C -40°C to +85°C -40°C to +85°C -40°C to +85°C -40°C to +85°C -40°C to +85°C -40°C to +85°C -40°C to +85°C | 8-Lead SOIC 8-Lead SOIC 8-Lead SOIC 8-Lead SOIC 8-Lead PDIP 8-Lead TSSOP 8-Lead TSSOP 8-Lead SOIC 8-Lead SOIC 8-Lead SOIC 8-Lead SOIC | R-8 R-8 R-8 R-8 N-8 RU-8 RU-8 R-8 R-8 R-8 R-8 | 2,500 2,500 1,000 1,000 2,500 1,000 |
| REF196GRU-REEL7 REF196GS REF196GS-REEL REF196GSZ-REEL7* | -40°C to +85°C -40°C to +85°C -40°C to +85°C -40°C to +85°C | 8-Lead TSSOP 8-Lead SOIC 8-Lead SOIC 8-Lead SOIC | RU-8 R-8 R-8 R-8 | 1,000 2,500 1,000 |
| REF198ES REF198ES-REEL REF198FS REF198FS-REEL REF198GP REF198GRU REF198GRU-REEL7 REF198GS REF198GS-REEL | -40°C to +85°C -40°C to +85°C -40°C to +85°C -40°C to +85°C -40°C to +85°C -40°C to +85°C -40°C to +85°C -40°C to +85°C -40°C to +85°C | 8-Lead SOIC 8-Lead SOIC 8-Lead SOIC 8-Lead SOIC 8-Lead PDIP 8-Lead TSSOP 8-Lead TSSOP 8-Lead SOIC 8-Lead SOIC | R-8 R-8 R-8 R-8 N-8 RU-8 RU-8 R-8 R-8 | 2,500 2,500 1,000 2,500 |

*Z = Pb-free part.

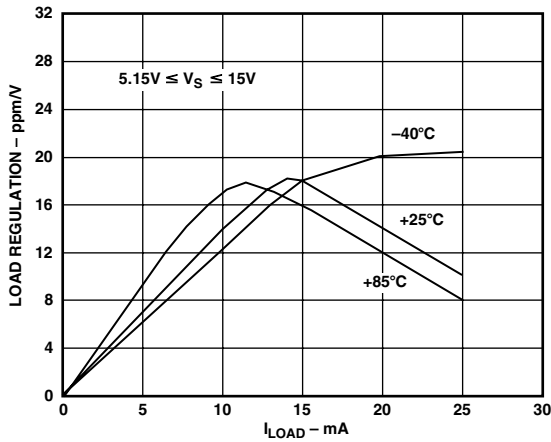
REF19x Series—Typical Performance Characteristics



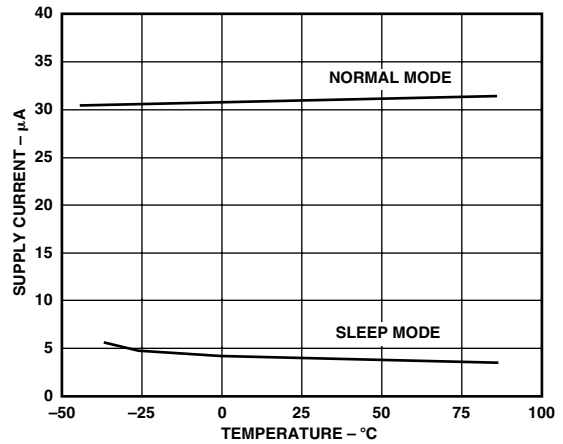
TPC 1. REF195 Output Voltage vs. Temperature



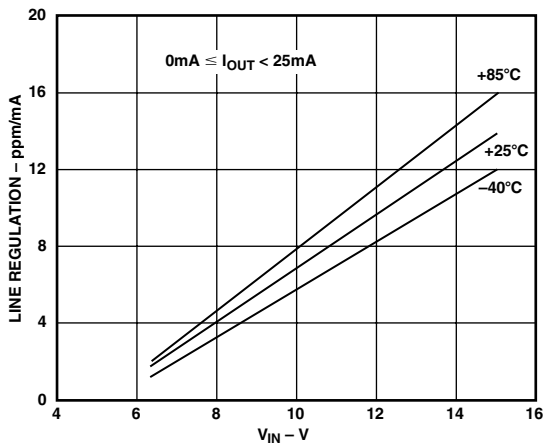
TPC 4. $T_C - V_{OUT}$ Distribution



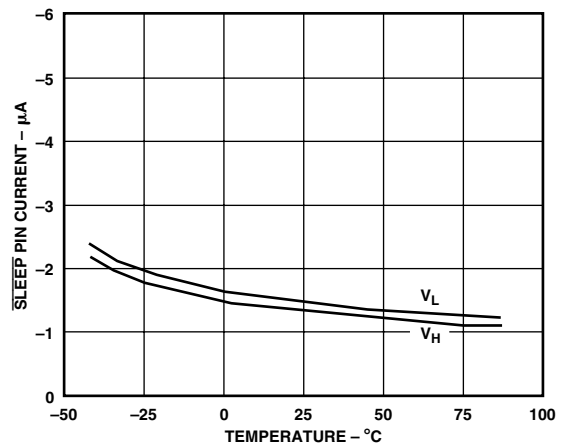
TPC 2. REF195 Load Regulation vs. I_{LOAD}



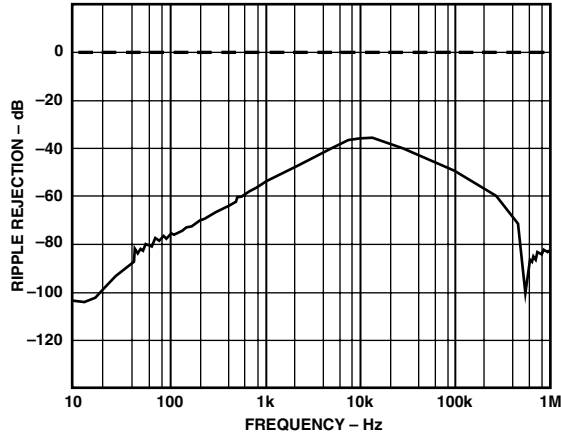
TPC 5. Quiescent Current vs. Temperature



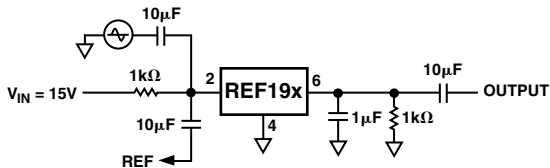
TPC 3. REF195 Line Regulation vs. V_{IN}



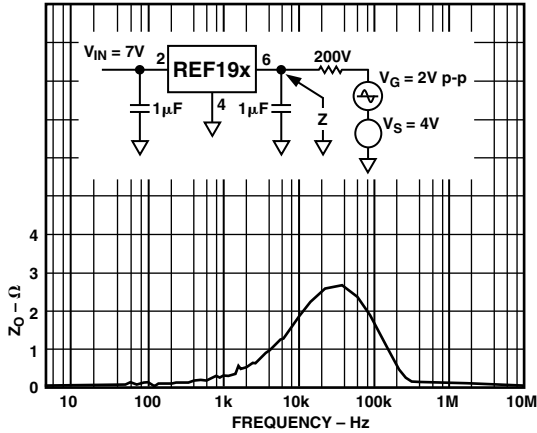
TPC 6. \overline{SLEEP} Pin Current vs. Temperature



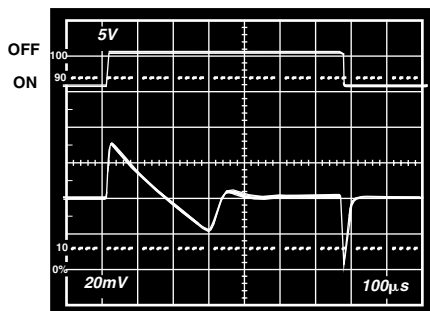
TPC 7a. Ripple Rejection vs. Frequency



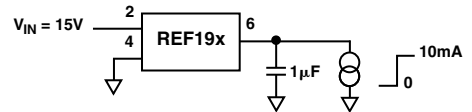
TPC 7b. Ripple Rejection vs. Frequency Measurement Circuit



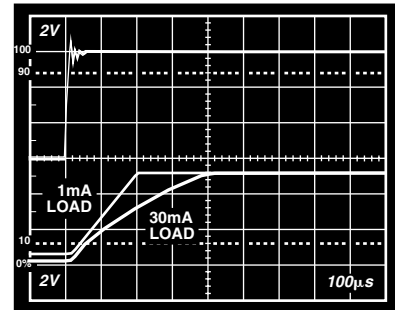
TPC 8. Output Impedance vs. Frequency



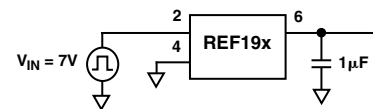
TPC 9a. Load Transient Response



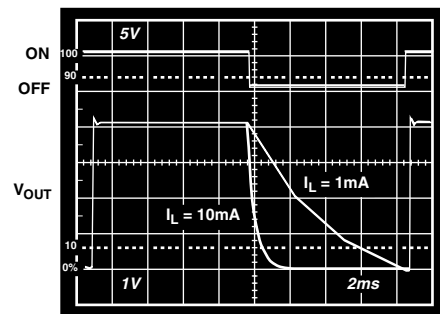
TPC 9b. Load Transient Response Measurement Circuit



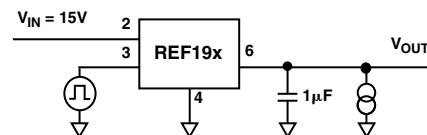
TPC 10a. Power ON Response Time



TPC 10b. Power ON Response Time Measurement Circuit

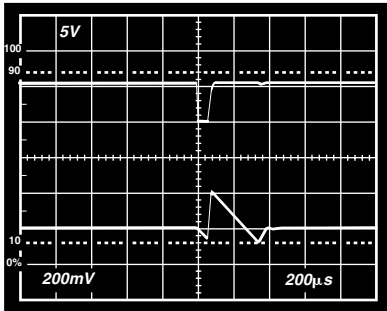


TPC 11a. SLEEP Response Time

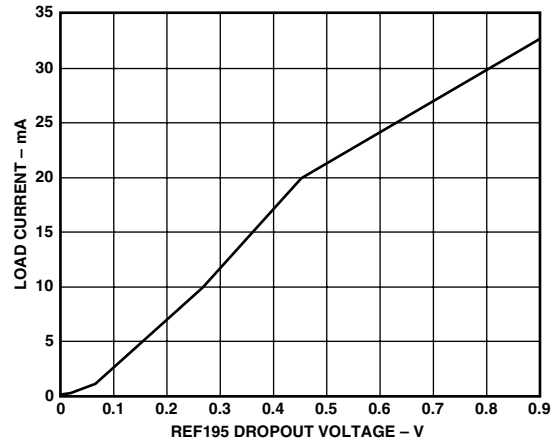


TPC 11b. SLEEP Response Time Measurement Circuit

REF19x Series



TPC 12. Line Transient Response



TPC 13. Load Current vs. Dropout Voltage

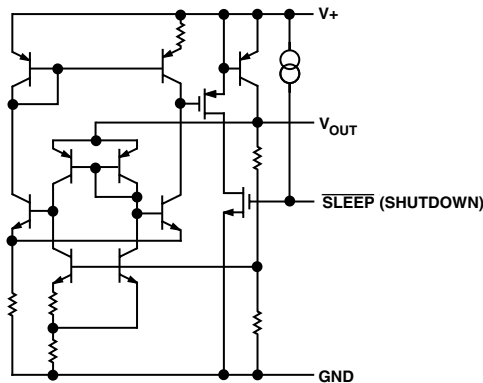


Figure 1. Simplified Schematic

APPLICATIONS SECTION

Output Short-Circuit Behavior

The REF19x family of devices is totally protected from damage due to accidental output shorts to GND or to V+. In the event of an accidental short-circuit condition, the reference device will shut down and limit its supply current to 40 mA.

Device Power Dissipation Considerations

The REF19x family of references is capable of delivering load currents to 30 mA with an input voltage that ranges from 3.3 V to 15 V. When these devices are used in applications with large input voltages, care should be exercised to avoid exceeding these devices' maximum internal power dissipation. Exceeding the published specifications for maximum power dissipation or junction temperature could result in premature device failure. The following formula should be used to calculate a device's maximum junction temperature or dissipation:

$$P_D = \frac{T_J - T_A}{\theta_{JA}}$$

In this equation, T_J and T_A are the junction and ambient temperatures, respectively, P_D is the device power dissipation, and θ_{JA} is the device package thermal resistance.

Output Voltage Bypassing

For stable operation, low dropout voltage regulators and references generally require a bypass capacitor connected from their V_{OUT} pins to their GND pins. Although the REF19x family of references is capable of stable operation with capacitive loads exceeding 100 μF , a 1 μF capacitor is sufficient to guarantee rated performance. The addition of a 0.1 μF ceramic capacitor in parallel with the bypass capacitor will improve load current transient performance. For best line voltage transient performance, it is recommended that the voltage inputs of these devices be bypassed with a 10 μF electrolytic capacitor in parallel with a 0.1 μF ceramic capacitor.

Sleep Mode Operation

All REF19x devices include a sleep capability that is TTL/CMOS level compatible. Internally, a pull-up current source to V_{IN} is connected at the SLEEP pin. This permits the SLEEP pin to be driven from an open collector/drain driver. A logic low or a 0 V condition on the SLEEP pin is required to turn off the output stage. During sleep, the output of the references becomes a high impedance state where its potential would then be determined by external circuitry. If the sleep feature is not used, it is recommended that the SLEEP pin be connected to V_{IN} (Pin 2).

Basic Voltage Reference Connections

The circuit in Figure 2 illustrates the basic configuration for the REF19x family of references. Note the 10 μF /0.1 μF bypass network on the input and the 1 μF /0.1 μF bypass network on the output. It is recommended that no connections be made to Pins 1, 5, 7, and 8. If the sleep feature is not required, Pin 3 should be connected to V_{IN} .

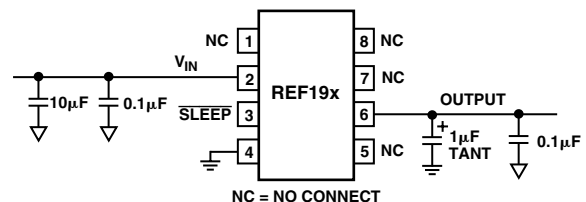


Figure 2. Basic Voltage Reference Configuration

Membrane Switch Controlled Power Supply

With output load currents in the tens of mA, the REF19x family of references can operate as a low dropout power supply in handheld instrument applications. In the circuit shown in Figure 3, a membrane ON/OFF switch is used to control the operation of the reference. During an initial power-on condition, the SLEEP pin is held to GND by the 10 kΩ resistor. Recall that this condition disables (read: three-state) the REF19x output. When the membrane ON switch is pressed, the SLEEP pin is momentarily pulled to V_{IN} , enabling the REF19x output. At this point, current through the 10 kΩ is reduced and the internal current source connected to the SLEEP pin takes control. Pin 3 assumes and remains at the same potential as V_{IN} . When the membrane OFF switch is pressed, the SLEEP pin is momentarily connected to GND, which once again disables the REF19x output.

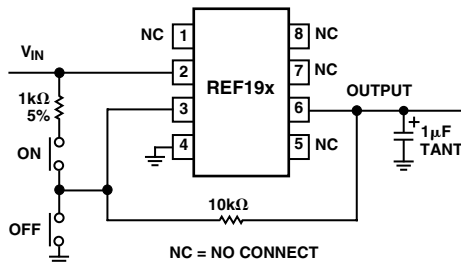


Figure 3. Membrane Switch Controlled Power Supply

Current-Boosted References with Current Limiting

While the 30 mA rated output current of the REF19x series is higher than typical of other reference ICs, it can be boosted to higher levels if desired with the addition of a simple external PNP transistor, as shown in Figure 4. Full-time current limiting is used for protection of the pass transistor against shorts.

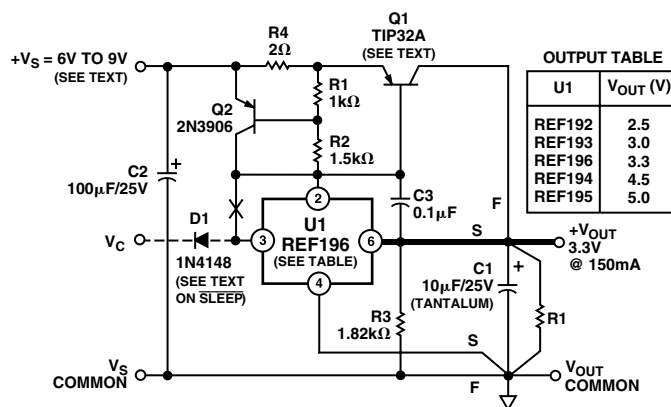


Figure 4. A Boosted 3.3 V Reference with Current Limiting

In this circuit, the power supply current of reference U1 flowing through R1 to R2 develops a base drive for Q1, whose collector provides the bulk of the output current. With a typical gain of 100 in Q1 for 100 mA to 200 mA loads, U1 is never required to furnish more than a few mA, so this factor minimizes temperature related drift. Short-circuit protection is provided by Q2, which

clamps drive to Q1 at about 300 mA of load current with values as shown. With this separation of control and power functions, dc stability is optimum, allowing best advantage use of premium grade REF19x devices for U1. Of course, load management should still be exercised. A short, heavy, low DCR (dc resistance) conductor should be used from U1 to 6 to the V_{OUT} sense point S, where the collector of Q1 connects to the load, point F.

Because of the current limiting configuration, the dropout voltage circuit is raised about 1.1 V over that of the REF19x devices, due to the V_{BE} of Q1 and the drop across current sense resistor R4. However, overall dropout is typically still low enough to allow operation of a 5 V to 3.3 V regulator/reference using the REF196 for U1 as noted, with a V_S as low as 4.5 V and a load current of 150 mA.

The requirement for a heat sink on Q1 depends on the maximum input voltage and short-circuit current. With $V_S = 5$ V and a 300 mA current limit, the worst-case dissipation of Q1 is 1.5 W, less than the TO-220 package 2 W limit. However, if smaller TO-39 or TO-5 packaged devices, such as the 2N4033, are used, the current limit should be reduced to keep maximum dissipation below the package rating. This is accomplished by simply raising R4.

A tantalum output capacitor is used at C1 for its low ESR (equivalent series resistance), and the higher value is required for stability. Capacitor C2 provides input bypassing and can be an ordinary electrolytic.

Shutdown control of the booster stage is shown as an option, and when used, some cautions are needed. Because of the additional active devices in the V_S line to U1, direct drive to Pin 3 does not work as with an unbuffered REF19x device. To enable shutdown control, the connection to U1 to U2 is broken at the X, and diode D1 then allows a CMOS control source V_C to drive U1 to 3 for ON/OFF operation. Startup from shutdown is not as clean under heavy load as it is in basic REF19x series and can require several milliseconds under load. Nevertheless, it is still effective and can fully control 150 mA loads. When shutdown control is used, heavy capacitive loads should be minimized.

A Negative Precision Reference without Precision Resistors

In many current-output CMOS DAC applications where the output signal voltage must be of the same polarity as the reference voltage, it is often required to reconfigure a current-switching DAC into a voltage-switching DAC through the use of a 1.25 V reference, an op amp, and a pair of resistors. Using a current-switching DAC directly requires an additional operational amplifier at the output to reinvert the signal. A negative voltage reference is then desirable because an additional operational amplifier is not required for either reinversion (current-switching mode) or amplification (voltage-switching mode) of the DAC output voltage. In general, any positive voltage reference can be converted into a negative voltage reference through the use of an operational amplifier and a pair of matched resistors in an inverting configuration. The disadvantage to that approach is that the largest single source of error in the circuit is the relative matching of the resistors used.

REF19x Series

The circuit illustrated in Figure 5 avoids the need for tightly matched resistors by using an active integrator circuit. In this circuit, the output of the voltage reference provides the input drive for the integrator. The integrator, to maintain circuit equilibrium, adjusts its output to establish the proper relationship between the reference's V_{OUT} and GND. Thus, any desired negative output voltage can be chosen by simply substituting for the appropriate reference IC. The sleep feature is maintained in the circuit with the simple addition of a PNP transistor and a 10 kΩ resistor. One caveat with this approach should be mentioned: although rail-to-rail output amplifiers work best in the application, these operational amplifiers require a finite amount (mV) of headroom when required to provide any load current. The choice for the circuit's negative supply should take this issue into account.

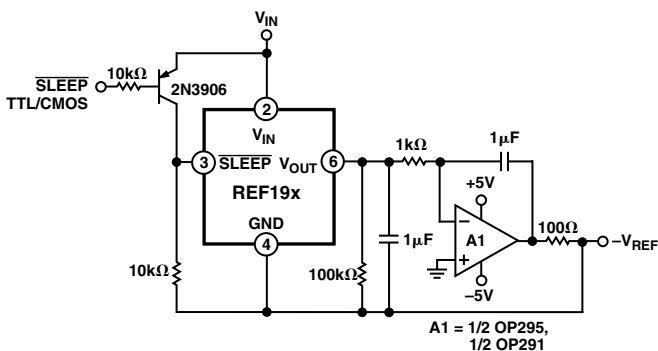


Figure 5. A Negative Precision Voltage Reference Uses No Precision Resistors

Stacking Reference ICs for Arbitrary Outputs

Some applications may require two reference voltage sources that are a combined sum of standard outputs. The circuit in Figure 6 shows how this stacked output reference can be implemented.

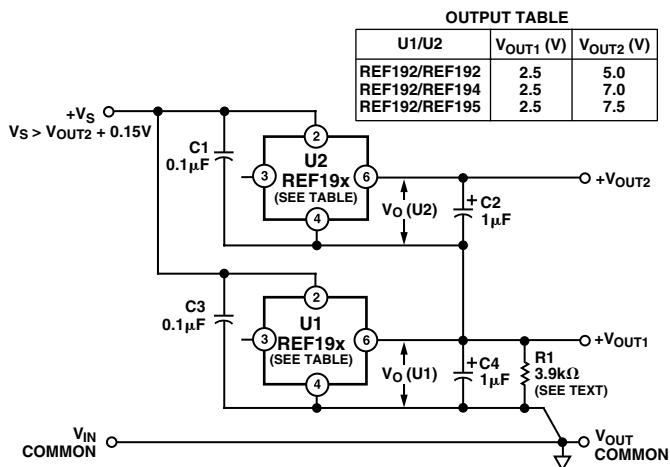


Figure 6. Stacking Voltage References with the REF19x

Two reference ICs are used, fed from a common unregulated input, V_S . The outputs of the individual ICs are simply connected in series as shown, which provides two output voltages, V_{OUT1} and V_{OUT2} . V_{OUT1} is the terminal voltage of U1, while

V_{OUT2} is the sum of this voltage and the terminal voltage of U2. U1 and U2 are simply chosen for the two voltages that supply the required outputs (see Table I). If, for example, both U1 and U2 are REF192s, the two outputs are 2.5 V and 5.0 V.

While this concept is simple, some cautions are needed. Since the lower reference circuit must sink a small bias current from U2 (50 μ A to 100 μ A), plus the base current from the series PNP output transistor in U2, either the external load of U1 or R1 must provide a path for this current. If the U1 minimum load is not well defined, Resistor R1 should be used, set to a value that will conservatively pass 600 μ A of current with the applicable V_{OUT1} across it. Note that the two U1 and U2 reference circuits are locally treated as macrocells, each having its own bypasses at input and output for best stability. Both U1 and U2 in this circuit can source dc currents up to their full rating. The minimum input voltage, V_S , is determined by the sum of the outputs, V_{OUT2} , plus the dropout voltage of U2.

A related variation on stacking two 3-terminal references is shown in Figure 6, where U1, a REF192, is stacked with a 2-terminal reference diode such as the AD589. Like the 3-terminal stacked reference above, this circuit provides two outputs, V_{OUT1} and V_{OUT2} , which are the individual terminal voltages of D1 and U1, respectively. Here this is 1.235 and 2.5, which provides a V_{OUT2} of 3.735 V. When using 2-terminal reference diodes, such as D1, the rated minimum and maximum device currents must be observed and the maximum load current from V_{OUT1} can be no greater than the current set up by R1 and $V_{O(U1)}$. In the case with $V_{O(U1)}$ equal to 2.5 V, R1 provides a 500 μ A bias to D1, so the maximum load current available at V_{OUT1} is 450 μ A or less.

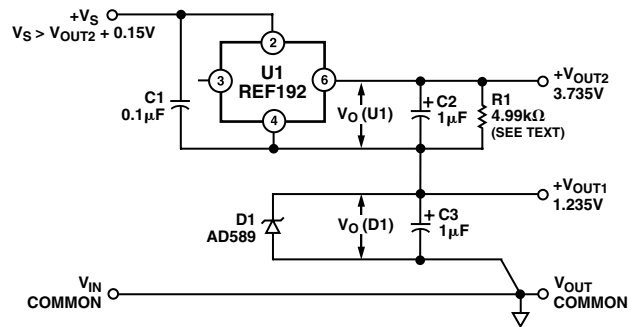


Figure 7. Stacking Voltage References with the REF19x

A Precision Current Source

Many times, in low power applications, the need arises for a precision current source that can operate on low supply voltages. As shown in Figure 8, any one of the devices in the REF19x family of references can be configured as a precision current source. The circuit configuration illustrated is a floating current source with a grounded load. The reference's output voltage is bootstrapped across R_{SET} , which sets the output current into the load. With this configuration, circuit precision is maintained for load currents in the range from the reference's supply current (typically, 30 μ A) to approximately 30 mA. The low dropout voltage of these devices maximizes the current source's output voltage compliance without excess headroom.

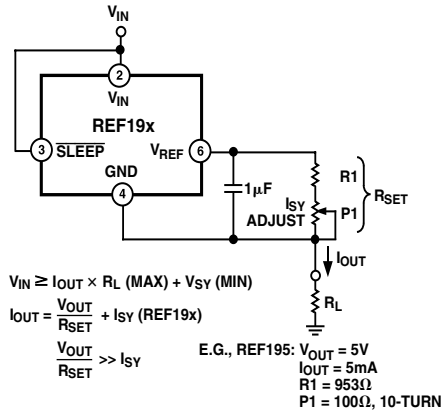


Figure 8. A Low Dropout, Precision Current Source

The circuit's governing equations are

$$V_{IN} = I_{OUT} \times R_L (Max) + V_{SY} (Min, REF19x)$$

$$I_{OUT} = \frac{V_{OUT}}{R_{SET}} + I_{SY} (REF19x)$$

$$\frac{V_{OUT}}{R_{SET}} \gg I_{SY} (REF19x)$$

Switched Output 5 V/3.3 V Reference

Applications often require digital control of reference voltages, selecting between one stable voltage and a second. With the sleep feature inherent to the REF19x series, switched output reference configurations are easily implemented with relatively little additional hardware.

The circuit of Figure 9 illustrates the general technique, which takes advantage of the output “wire-OR” capability of the REF19x device family. When OFF, a REF19x device is effectively an open circuit at the output node with respect to the power supply. When ON, a REF19x device can source current up to its current rating, but sink only a few μA (essentially just the relatively low current of the internal output scaling divider). As a result, for two devices wired together at their common outputs, the output voltage is simply that of the ON device. The OFF state device will draw a small standby current of 15 μA (max), but otherwise will not interfere with operation of the ON device, which can operate to its full current rating. Note that the two devices in the circuit conveniently share both input and output capacitors, and with CMOS logic drive, it is power efficient.

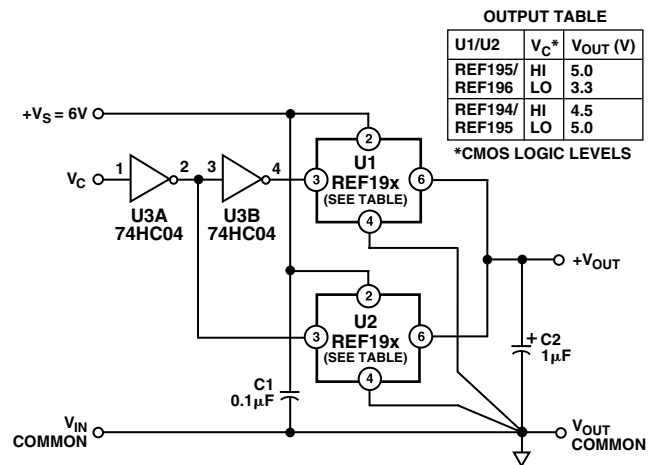


Figure 9. Switched Output Reference

Using dissimilar REF19x series devices with this configuration allows logic selection between the U1/U2 specified terminal voltages. For example, with U1 (a REF195) and U2 (a REF196), as noted in the table in Figure 9, changing the CMOS compatible V_C logic control voltage from HI to LO selects between a nominal output of 5.000 V and 3.300 V and vice versa. Other REF19x family units can also be used for U1/U2, with similar operation in a logic sense, but with outputs as per the individual paired devices (see table again). Of course, the exact output voltage tolerance, drift, and overall quality of the reference voltage will be consistent with the grade of individual U1 and U2 devices.

Because of the nature of the wire-OR, there is one application caveat that should be understood about this circuit. Since U1 and U2 can only source current effectively, negative going output voltage changes, which require the sinking of current, will necessarily take longer than positive going changes. In practice, this means that the circuit is quite fast when undergoing a transition from 3.3 V to 5 V, but the transition from 5 V to 3.3 V will take longer. Exactly how much longer will be a function of the load resistance, R_L , seen at the output and the typical 1 μF value of C2. In general, a conservative transition time here will be on the order of several milliseconds for load resistances in the range of 100 Ω to 1 k Ω . Note that for highest accuracy at the new output voltage, several time constants should be allowed (>7.6 time constants for <1/2 LSB error @ 10 bits, for example).

For V_S levels lower than the LOWER threshold, U3's output is low, thus U2 and Q1 are OFF, while U1 is ON. For V_S levels higher than the UPPER threshold, the situation reverses, with U1 OFF and both U2 and Q1 ON. In the interest of battery power conservation, all of the comparison switching circuitry is powered from V_S and is arranged so that when V_S fails, the default output comes from U1.

For the R1 to R3 values as shown, the LOWER/UPPER V_S switching thresholds are approximately 5.5 V and 6 V, respectively. These can obviously be changed to suit other V_S supplies, as can the REF19x devices used for U1 and U2, over a range of 2.5 V to 5 V of output. U3 can operate down to a V_S of 3.3 V, which is generally compatible with all family devices.

A Low Power, Strain Gage Circuit

As shown in Figure 12, the REF19x family of references can be used in conjunction with low supply voltage operational amplifiers, such as the OP492 and the OP283, in a self-contained strain gage circuit. In this circuit, the REF195 was used as the core of this low power, strain gage circuit. Other references can be easily accommodated by changing circuit element values. The references play a dual role as the voltage regulator to provide the supply voltage requirements of the strain gage and the operational amplifiers as well as a precision voltage reference for the current source used to stimulate the bridge. A distinct feature of the circuit is that it can be remotely controlled ON or OFF by digital means via the SLEEP pin.

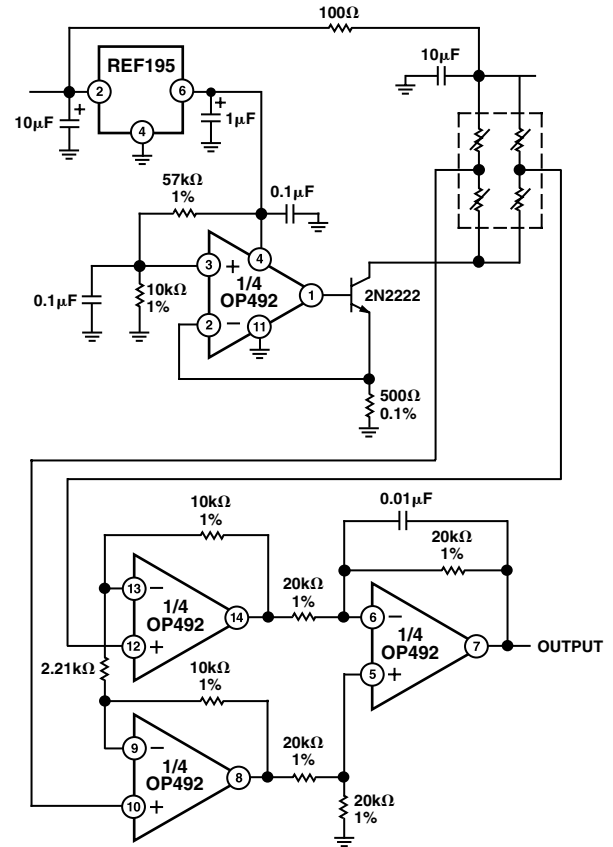


Figure 12. A Low Power, Strain Gage Circuit

REF19x Series

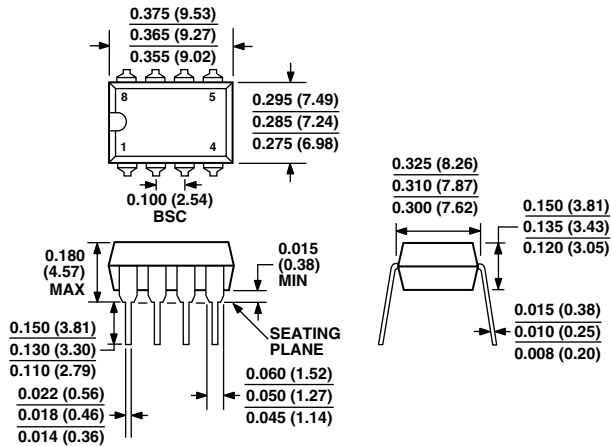
OUTLINE DIMENSIONS

8-Lead Plastic Dual In-Line Package [PDIP]

(N-8)

P-Suffix

Dimensions shown in inches and (millimeters)



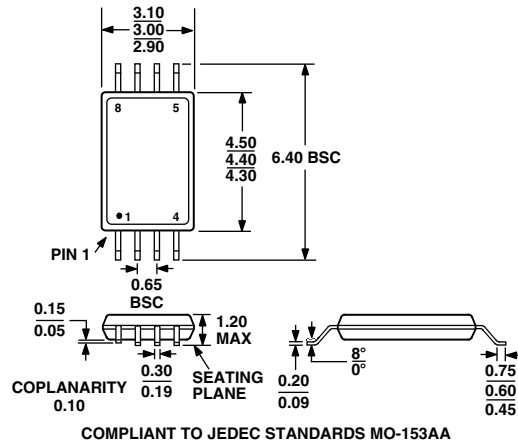
COMPLIANT TO JEDEC STANDARDS MO-095AA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Thin Shrink Small Outline Package [TSSOP]

(RU-8)

Dimensions shown in millimeters



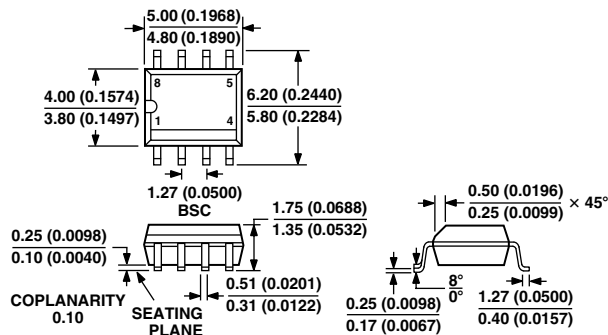
8-Lead Standard Small Outline Package [SOIC]

Narrow Body

(R-8)

S-Suffix

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

| Location | Page |
|---|------|
| 3/04—Data Sheet changed from REV. E to REV. F. | |
| Updated ABSOLUTE MAXIMUM RATINGS | 14 |
| Updated ORDERING GUIDE | 14 |
| Updated OUTLINE DIMENSIONS | 24 |
| 1/03—Data Sheet changed from REV. D to REV. E. | |
| Changes to TPCs 2 and 3 | 15 |
| Changes to Output Short Circuit Behavior | 17 |
| Changes to Figure 1 | 17 |
| Changes to Figure 5 | 19 |
| Updated OUTLINE DIMENSIONS | 23 |

